Nehalem-EX CPU Architecture
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NHM-EX Architecture
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Today’s Talk

• Nehalem-EX (NHM-EX) Processor Architecture
  – Focus on dataflow throughout the CPU
  – Focus on the bandwidth/latency/scalability aspects

• Things we are not disclosing today
  – Product clock Speeds
  – Detailed performance
  – Overall Intel Server Roadmap

• Minimize overlap with existing public information
  – Pointers to website links
Agenda: Building the Beast

- Start at the core and build outward
- Last Level Cache
- System Agent
- Coherence Agent
- Memory Controller
- System Interconnect
- Performance
- Conclusion
Tick-Tock Development Model

Merom
NEW Microarchitecture
65nm

Penryn
NEW Process
45nm

Nehalem
NEW Microarchitecture
45nm

Westmere
NEW Process
32nm

Sandy Bridge
NEW Microarchitecture
32nm

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All products, dates, and figures are preliminary and are subject to change without notice.

Nehalem-EX Architecture

Hot Chips 2009
Nehalem Core/Uncore Modularity

- Common core for client and server CPUs
  - Some unique features only on NHM-EX

- Uncore differentiates different segment specific CPUs
  - Scalable Core/Uncore gasket interface
  - Decouples core and uncore operation
Nehalem-EX CPU

- Monolithic single die CPU
- 8 Nehalem cores, 16 threads
- 24MB shared L3 cache
- 2 integrated memory controllers
- Scalable Memory Interconnect (SMI) with support for up to 8 DDR channels
- 4 Quick Path Interconnect (QPI) links with up to 6.4GT/s
- Supports 2, 4 and 8 socket in glueless configs and larger systems using Node Controller (NC)
- Intel 45nm process technology
- 2.3 Billion transistors
Cores and Last Level Caches

- Start with 8 Nehalem Cores
  - Modular and high throughput
  - 16 outstanding requests

- Large shared LLC
  - 24MB optimal mix of cache hierarchy capacity scaling as well as memory BW reduction

- Distributed, partitioned LLC for high BW
  - One cache slice per core
  - Multiple independent accesses in parallel
    - 4 per clock
  - PA hashed across slices to avoid hot-spots

- Inclusive LLC
  - Per-core valid bit tracks each line
  - Minimizes the amount of back snooping for last level cache WBs
  - Minimizes core snoops on external requests
  - Improves scalability and snoop latency
On-die network: Ring Interconnect

• High BW Ring Interconnect
  – Two counter rotating rings
  – Average latency ½ of unidirectional ring
  – 4X the BW of unidirectional ring
  – 4 protocol rings
    – Data ring 32Bytes in each direction

• Simple arbitration rules
  – Ring advances one stop per clock
  – “rotary rules”: traffic on the ring wins arbitration
  – Ring stops shared by core/cache
  – Ring stops tagged as “even”/”odd” polarities
  – Ring stops only sink from a single ring/polarity per cycle
  – Ring traffic injector responsible for polarity match at target polarity

• Scalable fabric
  – BW scales with ring stops
  – Simulated >250GB/s of interconnect BW
**QPI Caching agent**

- **Dual Caching agent**
  - QPI source snoop protocol
  - CA0/CA1 act as caching agent hubs to the rest of the system
    - QPI link layer end points
    - Processes inbound snoops
- **Local memory bypass**
  - Request to local memory controller
  - Direct fill to core for latency reduction
- **Supports high throughput**
  - 48 (96 total) requests outstanding.
  - All outstanding requests can be mapped to local socket
  - Up to 120 snoops buffered beyond QPI Link Layer

![QPI Caching agent diagram](image)
QPI Home Agent

- Dual Home agents
  - System coherence manager for memory associated with the adjacent memory controller
  - Tracks requests, resolves conflicts, returns memory data and completes transactions
  - Supports snoopy and hybrid coherence protocol.
    - IO agents tracked by in-memory directory

- Built to support large systems
  - Supports 256 outstanding requests
    - 48 requests from any single caching agent
  - Multiple modes for flexible topologies
    - Manages up to 8 other sockets and up to 4 IO/NC hubs

- Latency optimizations
  - Memory prefetch
  - Write-posting
Memory Controller and Memory subsystem

- Dual memory controllers
- Buffered interface
  - Two Scalable Memory Interface (SMI) interfaces per memory controller
    - Run in lockstep mode to minimize latencies & enable RAS
  - High speed serial links for maximum bandwidth (6:1 ratio)
  - Each channel connects to an Scalable Memory Buffer (SMB)
    - 2 DDR3 channels per buffer
    - Up to 4 DIMMs per buffer chip
- Large capacity/bandwidth per controller
  - Up to 16 DIMMS/64 Ranks per socket
  - Up to 8 DDR channels per socket
- Scheduler optimized for latency and BW
  - 32 (64 total) simultaneous requests can bid
  - Open, close and adaptive page policy
  - Out of order, rank granular scheduling
System Interconnect: Router and QPI

- Nehalem-EX supports 4 QPI link interfaces
  - High speed (6.4GT/s), packetized, P2P bidirectional link
  - Enables optimal, scalable and flexible system topologies
  - 25.6 GB/s of peak bandwidth per link

- Router glues external and internal interfaces
  - High BW, full crossbar connection with simultaneous 8 way routing
  - Route thru to support sparse topologies
  - Fully programmable routing capability for Efficient, flexible and broadcast messaging
  - Two deadlock free virtual channels to support complex deadlock free topologies
Nehalem-EX 4S Platform

Fully connected 4S system

- 1 link for the IO hub, 3 links for inter-socket
Platform Configurations

• Intel Architecture capable of QPI connected 8-Sockets / 128 threads

• Scalable systems and >8-socket capability with OEM node controllers

• Twisted Hypercube Interconnection

Max 2 QPI hops between two sockets
Nehalem-EX Performance

*Xeon® 5500 vs. Xeon® 5400*

- Up to **3.5x** Memory Bandwidth
- Up to **2.5x** Database Performance
- Up to **1.7x** Integer Throughput
- Up to **2.2x** Floating Point Throughput

*Nehalem-EX vs. Xeon® 7400*

- Up to **9x** Memory Bandwidth²
- **> 2.5x** Database Performance¹
- **> 1.7x** Integer Throughput
- **> 2.2x** Floating Point Throughput

*Expecting larger gains from Nehalem Architecture in MP*

¹Based on May’09 internal measurement using OLTP workload.
²Based on May’09 internal measurement using Intel internal workload
Nehalem-EX Summary

• Next generation of enterprise server CPU
• Focused on per socket throughput/bandwidth
  – 8 multi-threaded cores
  – Large LLC with high BW ring interconnect
  – Dual Caching agent, home agent/memory controllers
  – 4 high speed SMI memory links per socket
  – Support for large memory capacity

• Designed for highly scalable systems
  – Support high socket count as well as flexible MP configurations
  – 4 QPI links per socket
  – Large amount of on die buffering/queueing
Acknowledgements

“Beckton Team”