Transitioning the Intel® Next Generation Microarchitectures (Nehalem and Westmere) into the Mainstream

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Intel Corporation
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Agenda

• Next Generation Mainstream CPU’s
• New Technologies for Integration for 2009 and beyond
Intel® Core™ i7 Recap

• Core microarchitecture
  – Increased parallelism
    – e.g. 33% larger out of order window, handle more cache misses simultaneously
  – Enhanced algorithms
    – e.g. faster “unaligned” cache accesses, faster sync primitives, loop streaming detector, macro-fusion
  – Better branch prediction
    – e.g. 2nd level branch predictor, renamed RSB
  – New Instructions (SSE4)
  – Intel® Hyper-Threading Technology

• Uncore microarchitecture and connectivity
  – Scalable multi-core fabric
  – Shared last level Cache
  – Integrated memory controller
  – Intel® QuickPath Interconnect

• Power management technologies
  – PCU Microcontroller
  – Intel® Turbo Boost Technology
  – Integrated power gates
Enabling Nehalem for Every Segment

2008

- 4 Cores / 8 Threads
- 45 nm High-K
- Mainstream Desktop
- Thin & Light Laptop

2009+

- 2 Cores / 4 Threads with Integrated Graphics
- 32nm High-K
- Lynnfield
- Clarksfield
- Clarkdale
- Arrandale

Delivering Outstanding Nehalem Performance to Mainstream Desktops and Laptop Computers
Mainstream Platform Partitioning

Intel® Core™2 Processor based 3-Chip Solution

Nehalem/ Westmere based 2-Chip Solution

Greater Performance and Lower Power through Integration

1. Integrated graphics on Clarkdale/Arrandale

Intel® Microarchitecture codenamed Nehalem
Westmere: 32nm version of Intel® microarchitecture codename Nehalem
Mainstream Microprocessors

**Lynnfield/Clarksfield**

- 45nm processor (single die)
- DDR3
- Discrete Graphics
- 1x16 or 2x8, Gen2
- DMI
- Intel® 5 series Chipset
- Manageability, Security, Display, PCIe, SATA, etc.
Agenda

• Next Generation Mainstream CPU’s
• New Technologies for Integration for 2009 and beyond
**Integrated Power Gates**

- **Integrated Power Gates (switches)** are critical for integration, turning individual component blocks on/off
  - Zero leakage power, low latency to wake block
  - Key benefits in both idle and active power

- **Nehalem turns individual cores on/off**
  - Transparent to OS
  - Reduces latency to wake a core
  - Modular/Scalable Clocking
    - Cores, Memory System, I/O can run at independent voltage/frequency

- **Extended in 2009 platforms as Integrated Power Gates also used in shared cache and I/O logic to dynamically power down when inactive**

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**Integrated Power Gates enable Energy Efficient Integration**
Intel® Turbo Boost Technology

- Integration splits power allocation among more component blocks
- Intel® Turbo Boost Technology is critical to dynamically manage power allocation and seamlessly maximize performance
  - Higher benefits in smaller form factors

Dynamically Scaled Performance Boost
Intel® Hyper-Threading Technology

- Nehalem is a scalable multi-core architecture
- Hyper-Threading Technology augments benefits
  - Power-efficient way to boost performance in all form factors: higher multi-threaded performance, faster multi-tasking response

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Hyper-Threading

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<th>Shared or Partitioned</th>
<th>Replicated</th>
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<tr>
<td>Register State</td>
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<tr>
<td>Return Stack</td>
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<td></td>
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<tr>
<td>Reorder Buffer</td>
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<td>Instruction TLB</td>
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<tr>
<td>Reservation Stations</td>
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<tr>
<td>Cache (L1, L2)</td>
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<tr>
<td>Data TLB</td>
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<tr>
<td>Execution Units</td>
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Next generation Hyper-Threading Technology:
- Low-latency pipeline architecture
- Enhanced cache architecture
- Higher memory bandwidth

Enables 8-way processing in Quad Core systems, 4-way processing in Small Form Factors

Intel® Microarchitecture codenamed Nehalem
Energy Efficient Performance

- Many innovations in energy efficiency such as loop-streaming detector and dynamic loadline
- As looping is very common to every type of applications, Nehalem loop-streaming detector captures bigger loops and saves more energy

Dynamic only loadline (PCU)
- Power = Voltage x Current
- In prior processors, voltage line is anchored based on worst case
- Nehalem lowers Voltage based on current conditions: # active cores, temperature, and saves more energy.

Major Innovations in Energy Efficiency
Summary

• **Intel maintains pace of innovation and execution**
  – Next generation performance
  – 32nm: Another Process Technology Breakthrough

• **Enabling Nehalem for every segment**
  – Delivering outstanding Nehalem performance to mainstream desktops and laptop computers

• **Redesigning more efficient platforms**
  – Best performance across all segments
  – Low power and better power management
  – Higher levels of integration
Q & A
Lynnfield/ Clarksfield Microarchitecture

• Built on modularity of Intel® Core™ i7
• Further integration to support new mainstream platforms:
  – VTd and IO virtualization support
  – PCI Express* interface
    – x16 PCIe configurable to 2x8
    – 2.5 GT/s (Gen1) and 5 GT/s (Gen2)
    – Flexible interface: lane reversal, dynamic speed and link width changes, peer to peer posted writes
    – Power Optimization: L0s/L1 support, low-voltage swing mode and de-emphasis
  – x4 DMI Interface – Series 5 enhancements
  – Extended power management
Integrated Graphics and Media Architecture (Clarkdale, Arrandale)

- Unified Shader Architecture
  - Evolution of G965 & GM965
  - DX10 & Shader Model 4.0 in HW
  - Full HD Decode, High Quality Video
  - 6 threads/EU
  - Hierarchical Depth Buffer
- Dynamic load balanced
- Multi-functional; multi-threaded
- Enables scalability and flexibility
- Improved Extended Math, larger caches
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