Intel Xeon Accelerator Modules

Intel Front Side Bus FPGA Accelerators
The Industry’s only Xilinx Virtex-5 FSB Accelerator Module

- 64-bit 1066MHz FSB interface
- 8GB/s peak bandwidth
- 105ns host latency
- 256GB direct system memory access
- Intel MP platform compatible
- Modular product – optimization for different applications
- Xilinx Virtex-5 FPGA technology
- Supported by Intel QuickAssist AAL
- C → FPGA compiler support

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What is Intel QuickAssist?

- Comprehensive initiative that enables optimized use and deployment of accelerators (primarily FPGAs) on Intel platforms

QuickAssist Accelerator Abstraction Layer (AAL)

- Standard C/C++ API for inclusion with user application
- Device discovery support
- CPU initiated data transfer to FPGA (send data to accelerator)
- CPU initiated data transfer from FPGA (receive data back from accelerator)

Benefits

- Common software interface supporting multiple processing technologies
- Easy migration between different technologies and form factors
- Transparent – Open source approach
Intel’s Quickassist Accelerator Model

Accelerator Abstraction Layer

Application

Function Libraries (AFU Msgs)

Other Services (e.g. Config Database)

Device Services (e.g. Boot Loaders)

Function Libraries (AFU Msgs)

Common Function APIs e.g., MKL, IPP

Service APIs

Uniform Accelerator I/F

Accelerator Interface Adapters

Physical Interconnect

Accelerators

Common function library over FSB, QPI, PCIe or traditional IA based algorithms
Integrated Development Platform

- Pre-installed FPGA hardware
- Linux operating system
- Intel QuickAssist AAL
- VHDL IP cores
- Reference designs
- Documentation
- 1 year warranty
- 1 year technical support
- Optional design service assistance
Inside the 4U server

- IO Module
  - 2 + 2x Gbit NIC ports
  - Remote Management Module 2 Slot

- SAS Module with
  - Intel® Integrated RAID 0, 1, 1A, 5, 6, 10, 50, 60

- 5.25” Peripheral Device Bay

- DVD-ROM / CD-RW

- Hard Drives
  - 8 x 2.5” SAS/SATA Hot Swap

- Front Fan Module
  - Redundant Hot Swap

- PCIe (7 Slots)

- Rear Fan Modules
  - Redundant Hot Swap

- Memory Boards
  - 1 to 4 memory boards
  - FBD1 533/667
  - DIMM Slots (8 per brd)

- Quad-Core Intel® Xeon® Processors
  - 7300 Series (up to 4)

- Optional LCD Control Panel Shown
  - 3 front USB, 1 Video,
FSB Configuration Options

Intel’s Caneland MP Xeon platform

1x PCIe4 Slot

System Memory

21GB/s (peak)

4x PCIe8 Slots

North Bridge

2x PCIe8

4GB/s

switch

switch

2x PCIe4

Slots

South Bridge

FSB 8.5GB/s (peak)

4x SATA

User Defineable I/O
e.g. 60x 1GbE Ports

10GB/s

10GB/s

10GB/s

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FSB-Base Module

- **Compatible with Intel MP platforms**
  - Intel Xeon mPGA604 socket
  - Fits within Xeon heat sink footprint

- **Front Side Bus interface**
  - 64-bit 1066MHz
  - 8GB/s peak bandwidth*
  - 105ns latency
  - Direct access to system memory
  - Encrypted FSB core

- **Virtex-5 Interface/User FPGA**
  - FF1738 package, 42.5mm²
  - LX110-3

* 8GB/sec for 2 cache-line bursts
FSB-Compute Module

- **Virtex-5 User FPGAs**
  - Supports Largest LX or SX or FX FPGAs
  - Up to 207,360 LUT6’s
  - Up to 384 DSP48’s
  - Up to 1032 18Kbit Block Rams

- **4 independent banks of DDR-II SRAM**
  - 2 banks per FPGA
  - Up to 8MBytes per bank
  - 2x 32-bit data buses
  - 8GB/sec total bandwidth

- **Total Off Module B/W = 25.6GB/s**

- **Scalability**
  - Ability to stack multiple FSB-Compute modules

64 LVDS pairs = 6.4GB/sec

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FSB-Expansion Module

- **Virtex-5 User FPGA**
  - Supports Largest LX or SX or FX FPGA
  - >> 1TOP Fixed Precision/Bit Manipulation
  - Up to 100GF Single Precision FP
  - Up to 40GF Double Precision FP

- **4 banks of QDR-II SRAM**
  - Up to 16 MByte per bank
  - 16GB/sec total bandwidth

- **2 off-module GTP connectors**
  - 10 lanes @ 3.125Gbps per connector
  - 20 lanes total = 62.5 Gbps total

- **2 off-module digital connectors**
  - 40 pins per connector
  - Single-ended or LVDS I/O
  - E.g. For High Speed Video Capture
  - E.g. Ultra low latency, <20ns, point to point Comms

128 LVDS pairs = 12.8GB/sec

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Building the accelerator stack - 1

- **Intel Xeon Server Socket**
  - 73XX MP Xeon Series Compatible
  - MPGA-604 Socket
  - Zero Insertion Force Socket, ZIF
An Interposer is required to be fitted to the ZIF Socket
  - This provides the primary mating interface for the FPGA module stack.
- *FSB-BASE* module plugs directly into Intel Xeon socket
- Deals with low level FSB interface
- Referred to as the “Bridge” from the host to the user logic
Building the accelerator stack - 4

- Heatsink fitted to FSB interface FPGA
- ISI high density Custom Interconnect
  - 1526 pin HILO Connector
  - 0.8mm pitch
- Provides LVDS links to upper module(s)
Fits onto connectors of FSB-BASE module
- FSB-COMPUTE module #1 mates with connector
- Heatsinks applied to user FPGAs
Another ISI high density connector mates with FSB-COMPUTE #1 providing LVDS links to another upper module.
- FSB-COMPUTE #2 mates with the connector
- Heatsinks applied to user FPGAs
The final ISI high density connector provides another LVDS link.
The FSB-EXPANSION module mates with the connector, completing the stack of 5 Xilinx user FPGAs + FSB interface FPGA.
Heatsinks are fitted to user FPGA of FSB-Expansion module
The complete stack...
- Raw Compute Performance
  - > 500GF SPFP
  - > 200GF DPFP
  - >> 5TOPs Integer / Bit Manipulation
- Power Consumption
  - Up to 130 Watts Maximum
  - 24 Watts Max per FPGA/Memory
- Stack is currently factory configured
  - Updating for Customer Configuration
    - Insertion / Extraction Tool
    - Calibration Software
Stack Level Functional Block Diagram

64 LVDS pairs @ 800MHz = 6.4GB/sec
Latency = 20ns

128 LVDS pairs @ 800MHz = 12.8GB/sec
Latency = 20ns

64-bit/1,066MHz Front Side Bus

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Thank You

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