Newest Additions to Altera’s Integrated Transceiver Portfolio

Stratix IV GT FPGA
Integrated 11.3Gbps Transceivers

Arria II GX FPGA
Integrated 3.75Gbps Transceivers

Dan Mansur, Altera Corporation
Stratix IV GT FPGA – Shipping 1Q09

40nm
2.5 Billion Transistors
11.3Gbps Transceivers
Broadest Integrated Transceiver Portfolio

Transceiver speeds from 155 Mbps – 11.3 Gbps

Maximum Transceiver Data Rate

3.75 Gbps  8.5 Gbps  11.3 Gbps

Low Power  Low Cost

11.3 Gbps Transceivers
Stratix IV GT FPGA

- First 40nm FPGA available with 11.3 Gbps transceivers
  - Shipping today, both 230K and 530K equivalent LE (logic elements or 4 input look-up-table equivalent)
  - Up to 48 transceivers, 24 running at 11.3 Gbps
  - Superior signal integrity, meets XLAUI/CAUI, CEI-11G specifications

- Optimized to meet 40G/100G system requirements
  - Highest density with lowest power
  - Core performance to match 100G requirements
  - Interoperability testing with optical module vendors
  - Integrated transceivers, no external 10G PHY required

- IP & board solutions
  - Reliable 3rd party IP solutions available now
  - Signal Integrity board available for evaluation of transceivers
  - 100G demonstration platform available July, 2009
# Stratix IV GT FPGA Device Family

<table>
<thead>
<tr>
<th>Device</th>
<th>LEs</th>
<th>Transceivers 11.3, 8.5, 6.5 Gbps (Total)</th>
<th>LVDS</th>
<th>I/Os</th>
<th>Memory (Mbits)</th>
<th>Package¹</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>40G Devices</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP4S40G2</td>
<td>230K</td>
<td>12, 12, 12 (36)</td>
<td>44</td>
<td>636</td>
<td>13.9</td>
<td>F1517</td>
</tr>
<tr>
<td>EP4S40G5</td>
<td>530K</td>
<td>12, 12, 12 (36)</td>
<td>44</td>
<td>636</td>
<td>20.3</td>
<td>H1517</td>
</tr>
<tr>
<td><strong>100G Devices</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP4S100G2</td>
<td>230K</td>
<td>24, 0, 12 (36)</td>
<td>44</td>
<td>636</td>
<td>13.9</td>
<td>F1517</td>
</tr>
<tr>
<td>EP4S100G5</td>
<td>530K</td>
<td>24, 0, 12 (36)</td>
<td>44</td>
<td>636</td>
<td>20.3</td>
<td>H1517</td>
</tr>
<tr>
<td>EP4S100G3</td>
<td>290K</td>
<td>24, 8, 16 (48)</td>
<td>44</td>
<td>754</td>
<td>13.3</td>
<td>F1932</td>
</tr>
<tr>
<td>EP4S100G4</td>
<td>360K</td>
<td>24, 8, 16 (48)</td>
<td>44</td>
<td>754</td>
<td>17.7</td>
<td>F1932</td>
</tr>
<tr>
<td>EP4S100G5</td>
<td>530K</td>
<td>24, 8, 16 (48)</td>
<td>44</td>
<td>754</td>
<td>20.3</td>
<td>F1932</td>
</tr>
</tbody>
</table>

Note 1: Flip chip ball-grid array (BGA) with 1.0-mm pitch

H = Hybrid package

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Stratix IV GT FPGA TX Eye Diagram, 11.3 Gbps

- Superior jitter performance
  - Wide open TX eye, 8 channels switching at 11.3 Gbps
Stratix IV GT FPGA Jitter Tolerance, 11.3 Gbps

EP4S100G2F40 Receiver CDR Jitter Tolerance

Data Rate = 11.3 Gbps, Reference Clock Frequency = 565 MHz
PRBS-31, BER = 10^{-12}, 95% Confidence Level

BERT maximum sinusoidal jitter amplitude limit = 12.43 UI

- Exceeding CEI-11G SR jitter tolerance with margin
Showing SFP+ Module Interoperability

- EP4S100G2, ES1 device
- Room temperature
- 6 transceiver channels active
- 1 transceiver channel observed
- PRBS 31 data pattern
- Vod = 600mV
- Pre-emphasis setting = 5

- Far end eye-diagram, Avago SFP+ SR optical module, 10.3125 Gbps
- Eye wide open after 100m multi-mode fiber (MMF) optical loopback
# Stratix IV GT FPGA 10/40/100G Protocols

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Interface</th>
<th>Number of lanes per side</th>
<th>Data rates</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>10G independent channels</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10Gb Ethernet, 10Gb Fibre Channel</td>
<td>XFI, SFI (1)</td>
<td>1-12</td>
<td>10.3, 10.7 Gbps</td>
</tr>
<tr>
<td>Sonet/SDH OC-192/STM-64, G.709 OUT-2</td>
<td>XFI, SFI (1)</td>
<td>1-12</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td>10G Basic (Proprietary)</td>
<td>OIF/CEI-11G</td>
<td>1-12</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td><strong>40G bonded channels</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interlaken</td>
<td>OIF/CEI-6G</td>
<td>8-12</td>
<td>4.976–6.375 Gbps</td>
</tr>
<tr>
<td>SPAUI, DDR-XAUI</td>
<td>OIF/CEI-6G</td>
<td>2-6</td>
<td>6.4 Gbps</td>
</tr>
<tr>
<td>40G IEEE 802.3ba</td>
<td>XLAUI</td>
<td>4</td>
<td>10.3125 Gbps</td>
</tr>
<tr>
<td>SFI-4.2</td>
<td>SXI-5</td>
<td>5</td>
<td>2.488–3.125 Gbps</td>
</tr>
<tr>
<td>SFI-5.1</td>
<td>SXI-5</td>
<td>17</td>
<td>2.488–3.125 Gbps</td>
</tr>
<tr>
<td>SFI-5.2</td>
<td>OIF/CEI-11G</td>
<td>5</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td>SFI-S</td>
<td>OIF/CEI-11G</td>
<td>5</td>
<td>9.9–11.3 Gbps</td>
</tr>
<tr>
<td><strong>100G bonded channels</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interlaken</td>
<td>OIF/CEI-6G</td>
<td>20-24</td>
<td>4.976–6.375 Gbps</td>
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<td>SPAUI, DDR-XAUI</td>
<td>OIF/CEI-6G</td>
<td>4-6</td>
<td>6.4 Gbps</td>
</tr>
<tr>
<td>100G IEEE 802.3ba</td>
<td>CAUI</td>
<td>10</td>
<td>10.3125 Gbps</td>
</tr>
<tr>
<td>SFI-S</td>
<td>OIF/CEI-11G</td>
<td>11</td>
<td>9.9–11.3 Gbps</td>
</tr>
</tbody>
</table>

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Note 1. Support for SFI-S may require external signal conditioning (EDC) chip

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Example: 100G Line Card

1. 100G chip-to-backplane
   Example
   SPAUI and DDR-XAUI

2. 100G chip-to-chip
   Example
   Interlaken 20-24 @ 6.375 Gbps

3. 100G chip-to-module
   Example
   CAUI (10 lanes @ 10G)

Switch fabric/backplane

Fabric Manager

100G MAC Packet Processing

100G = 9.9 – 11.3 Gbps
Example: 100G OTN4

1. 100G Module Interface Example
   SFI-S/MLD (10 @ 11.3 Gbps)

2. 100G Chip-Chip SFI-S @ 10 Gbps

3. 100G Module Interface Example
   SFI-S/MLD (10 @ 11.3 Gbps)

Line/ optical module

1

ALERTA

Stratix IV GT

Client interface Ethernet MAC

2

线 optical module

2

ALERTA

Stratix IV GT

Line interface OTN4 framer/mapper

3

ALERTA

Stratix IV GT

FEC encode/ decode

10G = 9.9 – 11.3 Gbps

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Arria II GX FPGA – Low Cost Transceiver FPGA with High-End Capabilities

- **Low cost**
  - $15 entry price: EP2AGX20, 100K units in 2011
  - Half the price of competing high-end FPGAs

- **High functionality**
  - High-performance ALM-based fabric
  - High density - up to 260K LEs
  - Up to 16 transceivers @ 3.75 Gbps
  - Up to 12 Mbits of memory
  - Highest ratio of DSP-to-logic resources in its class

- **Low power**
  - Up to 50% lower power than competing high-end FPGAs
  - <100mW per transceiver channel @ 3.125 Gbps
## Arria II GX FPGA Family Plan

<table>
<thead>
<tr>
<th>Device</th>
<th>Equiv LEs</th>
<th>RAM Mbits/ M9K blocks</th>
<th>Total MLAB memory (Mbits)</th>
<th>18 X 18 multipliers</th>
<th>Transceivers @ 3.75 Gbps</th>
<th>PLLs</th>
<th>Tx PLLs</th>
<th>Clks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP2AGX20</td>
<td>16K</td>
<td>0.7 / 87</td>
<td>0.4</td>
<td>56</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>32</td>
</tr>
<tr>
<td>EP2AGX30</td>
<td>27K</td>
<td>1.3 / 144</td>
<td>0.5</td>
<td>144</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>32</td>
</tr>
<tr>
<td>EP2AGX45</td>
<td>45K</td>
<td>2.9 / 319</td>
<td>0.6</td>
<td>228</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>32</td>
</tr>
<tr>
<td>EP2AGX65</td>
<td>63K</td>
<td>4.4 / 495</td>
<td>0.8</td>
<td>312</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>32</td>
</tr>
<tr>
<td>EP2AGX95</td>
<td>94K</td>
<td>5.5 / 612</td>
<td>1.2</td>
<td>448</td>
<td>12</td>
<td>6</td>
<td>6</td>
<td>40</td>
</tr>
<tr>
<td>EP2AGX125</td>
<td>124K</td>
<td>6.6 / 730</td>
<td>1.6</td>
<td>576</td>
<td>12</td>
<td>6</td>
<td>6</td>
<td>40</td>
</tr>
<tr>
<td>EP2AGX190</td>
<td>190K</td>
<td>7.6 / 840</td>
<td>2.4</td>
<td>656</td>
<td>16</td>
<td>6</td>
<td>8</td>
<td>40</td>
</tr>
<tr>
<td>EP2AGX260</td>
<td>256K</td>
<td>8.5 / 950</td>
<td>3.2</td>
<td>736</td>
<td>16</td>
<td>6</td>
<td>8</td>
<td>40</td>
</tr>
</tbody>
</table>
## Arria II GX FPGA Package Offerings

<table>
<thead>
<tr>
<th>Device</th>
<th>U358</th>
<th>F572</th>
<th>F780</th>
<th>F1152</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.8 mm 17 x 17</td>
<td>1.0 mm 25 x 25</td>
<td>1.0 mm 29 x 29</td>
<td>1.0 mm 35 x 35</td>
</tr>
<tr>
<td>EP2AGX20</td>
<td>156 (32,4)</td>
<td>252 (56,4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP2AGX30</td>
<td>156 (32,4)</td>
<td>252 (56,4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP2AGX45</td>
<td>156 (32,4)</td>
<td>252 (56,8)</td>
<td>364 (84,8)</td>
<td></td>
</tr>
<tr>
<td>EP2AGX65</td>
<td>156 (32,4)</td>
<td>252 (56,8)</td>
<td>364 (84,8)</td>
<td></td>
</tr>
<tr>
<td>EP2AGX95</td>
<td>260 (56,8)</td>
<td>372 (84,12)</td>
<td>452 (104,12)</td>
<td></td>
</tr>
<tr>
<td>EP2AGX125</td>
<td>260 (56,8)</td>
<td>372 (84,12)</td>
<td>452 (104,12)</td>
<td></td>
</tr>
<tr>
<td>EP2AGX190</td>
<td></td>
<td>372 (84,12)</td>
<td>612 (144,16)</td>
<td></td>
</tr>
<tr>
<td>EP2AGX260</td>
<td></td>
<td>372 (84,12)</td>
<td>612 (144,16)</td>
<td></td>
</tr>
</tbody>
</table>

Number of I/Os (LVDS, number of transceivers)
Example: Remote Radio Head

- Lowest power possible (<5W)
- 1-200K LEs
- 6-10 Mbits internal memory
- 500 18x18 multipliers
- ~250-MHz operating frequency
- Transceivers for CPRI and GE
Quartus II Software Innovations

- Incremental compilation
  - Increase team productivity through support for team-based design flows using top-down or bottom-up methodologies

- Multi-processor support
  - Get faster compilation times (30% with 4 processors) with multi-processor systems

- TimeQuest timing analyzer
  - Close timing faster with the easy-to-use with SDC support

- PowerPlay technology
  - Automatically optimizing your design for low power

- SOPC Builder
  - Improve productivity with automatic integration of your intellectual property (IP) cores and user components

- SignalTap® II logic analyzer
  - Shorten verification cycles with in-system debugging of your design

- Low memory usage
Example: Parallel Synthesis Speed-up

- **Definition of parallel compilation**
  - The use of multiple processors or multi-cores on a single computer during compilation

- **Parallel synthesis during incremental compilation**
  - Design must contain partitions (QIC)
    - Partitions are synthesized in parallel
  - *Off* by default

<table>
<thead>
<tr>
<th># Processors</th>
<th>Map 1.4x</th>
<th>Total Flow 1.9x</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Compile Time Speed-up</th>
<th>1.4x</th>
<th>1.9x</th>
<th>1.1x</th>
<th>1.16x</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Working Set *</td>
<td>1.6x</td>
<td>2.3x</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Set of memory pages recently touched by threads in the process
Summary

- **Stratix IV GT FPGA = Highest Bandwidth**
  - 11.3Gbps 48 transceivers
  - 1~1.6Gbps 900 user IO
  - 1,300 RAM blocks

- **Arria II GX FPGA = Low-Cost Transceiver FPGA with High-End Capabilities**
  - ½ Watt and $15.00
  - 3.75Gbps 16 transceiver
  - 800MHz 600 user IO
  - 950 RAM blocks