Stratix® 10:
14nm FPGA Delivering 1GHz

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Stratix 10 Architectural Big Rocks

- 2X the achievable performance of Stratix V
- At up to 70% lower power
- Heterogeneous 3D System In Package (SiP) integration
- Adoption of Intel 14nm tri-Gate process
- Hierarchical configuration and security
Stratix 10 Innovations: 2.5D

- Multi-Die via EMIB
  - Separate core / transceiver
  - Embedded Multi-Die Interconnect Bridge

FPGA Core Die
Stratix 10 Innovations: Configuration & Clocking

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  - Separate core / transceiver
  - Embedded Multi-Die Interconnect Bridge

- Scalable Sector Architecture
  - Software Configuration
  - Configuration NoC
  - Routable Clocks
Stratix 10 Innovations: HyperFlex

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- Scalable Sector Architecture
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  - Routable Clocks

- Core Performance
  - HyperFlex Fabric, Tri-Gate
  - 1GHz M20K and DSP MAC
  - 750 MHz Floating Point
Stratix 10 Innovations: SoC & Memory

- Multi-Die via EMIB
  - Separate core / transceiver
  - Embedded Multi-Die Interconnect Bridge

- Scalable Sector Architecture
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- SoC
  - 1.5GHz Performance ARM® Cortex A53
  - DDR I/O Banks with Hard Memory Controller
System-in-Package Construction

XCVR (6CH)

PCIe x16

XCVR (6CH)

XCVR tile

24 XCVRs

PCIe HIP

3V GPIO

XCVR (6CH)

Core Fabric

Note: Not to-scale
System-in-Package EMIB Technology

Many benefits

- Reduced complexity vs. full interposer, and no reticle limit
- De-Couple analog (transceiver) development from digital FPGA fabric
- Transceiver reliability & yield enhancement
  - Don’t need rectangular “die”
  - Matching transceiver speed-grades
- Tick mixed with tock for added derivatives
  - E.g. 56G PAM4 transceiver tile
  - E.g. new hardened I/O interface IP
  - E.g. SiP Memory or ASIC tiles
Sectors and Configuration Sub-System

- Config-System manages CRAM
- Historically just a shift register
  - AR/DR to Configuration RAM Array
  - FSM controlled

- Modern configuration adds significant system functionality
  - Encryption, decryption, bitstream compression, redundancy
  - Security: authentication, side-Channel, firewall, PUF
  - SEU, scrubbing and partial-configuration management
  - Debug

- Our solution: move it to software
  - More robust, upgradable, and risk-averse
Stratix 10 Configuration Sub-system Overview

- **Secure Device Manager (SDM)**
  - Config and Re-Config, compression
  - Security: authentication, encryption, PUF
  - Maintenance (power, T/V, SEU, debug)

- **Local Sector Manager (LSM)**
  - Sector configuration manager

- **Config Network-on-Chip (CNoC)**
  - SDM/LSM Communication

![Diagram of SDM and CNoC](image-url)
SoC Application Processor

1.5 GHz Quad-Core ARM® Cortex™ A53
- CCU: Cache-coherency between FPGA accelerators and processors
- Integrated with configuration subsystem (SDM) – sharing peripherals
Routable Clocking

- SW-routed clocks in sector “seams”
- More efficient use of globals
- Active skew management

(Legacy) Global Spines

Stratix 10 Routed Clocks
Core Fabric Building Blocks

Adaptive Logic Module

20Kb

1GHz RAM
Data Forwarding

1GHz DSP MAC
10 TFLOPs IEEE 754

LAB clusters, staggered H/V routing

LIM/LEIM/DIM fabric
Fabric Performance and Power

Performance:
- A complete “re-think” on the philosophy of FPGA Fabric Architecture
- Registers are not just logic resources, they are routing resources
- Goal is to enable seamless movement and addition (pipelining) of registers
- **Target**: 2X the performance, without making the wires “2x faster”

Power
- 14nm Tri-Gate process (FinFET) provides process benefit for power
- Expanded use of VID and power management adds more
  - High-Performance 800 mV to 940 mV
  - Low-Power options from 850 mV down to 800 mV
- HyperFlex for power reduction
  - Combine performance from HyperFlex with low-power options
- **Target**: 50% to 70% lower power per function, without slowing down
Re-timing and Pipelining in Conventional FPGAs

Re-Timing
- Balance flops
- 16% $f_{\text{max}}$ gain
- Added area

Raw Logic
- Unbalanced paths

Pipelining
- Add flops
- 40% $f_{\text{max}}$ gain
- Added clock tick
- Added area
Routing muxes (all H/V wires) have optional registers
- Including LAB, M20K and DSP block inputs, CC, SCLR/CE

Architectural Goals:
- Perfect balance – P&R chooses the right register (of many) to turn on
- Simple Software – Re-timing is a simple push/pull along the path
- No wasted LEs – Designs with high FF:LUT ratios no longer an issue
- No wasted routing – Don’t have to route to find an available FF
Moving a Register in the HyperFlex fabric

- Disable in ALM, add to routing

- Moving a register is a push/pull operation on the route
- There is always a register on the routing mux
- Quartus® II chooses the most appropriate FF for path balancing
Re-timing and Pipelining in Stratix 10

Re-Timing
- Balance flops
- 40% $f_{\text{max}}$ gain
- Same resources

Pipelining
- Add flop
- Add clock tick
- 2X $f_{\text{max}}$ gain
- Same resources
Software and Designer Use-Model

- Software adds a new step

- Designer/SW concentrate on critical *domains/chains*, not volatile reg-reg paths

- HyperPipeline the data-path, optimize control logic
Power: Half the power per function

- 14nm Tri-Gate provides a good chunk of this
  - Allows us to take more of the process benefit as performance

- Expanded use of VID and power management
  - M20K and DSP block power gating

- Added registers helps:
  - Reduced footprint for register-heavy designs

- At 2X the speed, reduced size
  - Half the width means half the area
  - Which means half the static power on the same device.
Area/Delay/Power Tradeoffs with Stratix 10

Stratix V Migrate to Stratix 10

- ½ Width
- 2x f_max
- 2X Throughput

Power

Stratix V

Migrate to Stratix 10

AC

DC

I/O
Summary

- 3D integration isn’t just integration, it is
  - De-risking, process matching, derivative proliferation and tick/tock
- Device floorplanning and configuration get an upgrade
  - Software control allows for security and feature-up of devices
- SoC integration is mainstream
  - Processor cost is a small subset of the die, coherent-accelerators
- Pipelining unlocks optimizations in FPGA architecture
  - Using wires efficiently, not brute-forcing them faster
  - Faster == lower power when you can get designs to a more efficient place
- Process is still giving us power benefits
  - 14nm Tri-Gate reduces power, enabling higher performance circuit-design
Thank You