Memory as We Approach a New Horizon

Hot Chips 2016 Memory Tutorial

J. Thomas Pawlowski, Chief Technologist, Fellow
Outline

- Micron Overview
- Memory technology scaling
- DRAM then and now
- Seeking high bandwidth
- Persistent memory
- The future: additional classes of bits
Micron by the Numbers

37 Years strong in

20 Countries with 13 Manufacturing and R&D sites,

30,000+ Team Members and

Net Sales in 2015 of

$16,100,000,000
Micron’s Comprehensive Memory Portfolio
OFFERING THE BROADEST AND MOST ADVANCED SOLUTIONS - INDUSTRY STANDARD AND DIFFERENTIATED
Unprecedented Data Growth Driving System Evolution

Networking
60% more traffic per year with 30% less energy

Cloud/Big Data
44 zettabytes of stored data

IoT
50 billion connected devices in 2020

Mobile/Client
38 exabytes of traffic per year, driven by video/photos/apps

Enterprise
OLTP systems with low-latency in-memory compute

Autonomous
Customer-ready autonomous vehicles by 2020

Sources: Gartner, Cisco Visual Networking Index, European Commission, HP.com
DRAM Scaling Continues with Increasing Complexity

- Large increase in number of process steps to enable shrink
- Conversion Capital Expenditure scales with number of steps
- Significant reduction in wafer output per existing cleanroom area

<table>
<thead>
<tr>
<th>Complexity Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>50nm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th># Mask Levels</th>
<th># non-Litho Steps per Critical Mask Level</th>
<th>Cleanroom Space per Wafer Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>~10%</td>
<td>~40%</td>
<td>~15%</td>
</tr>
<tr>
<td>&gt;35%</td>
<td>&gt;110%</td>
<td>&gt;80%</td>
</tr>
</tbody>
</table>

Steps of ~100% bits/wafer increase
3D NAND versus Planar NAND Scaling

- **Planar NAND scaling**
  - Planar can be scaled below 16nm, but performance and cost are not competitive with 3D NAND
  - Micron focused 100% on 3D NAND after 16nm

- **3D NAND scaling**
  - 3D NAND cost/capacity improvement over planar expands with subsequent nodes
  - 3D NAND cell architecture enables significant performance improvement relative to planar technology
DRAM Then and Now

- Traditional high volume DRAM, mainly module form 64b combined data bus
  - ~doubling bandwidth with each architecture, mainstream ranges:
    - FPM 177MB/s  EDO 266MB/s  SDR 533-1066MB/s 3.3V 1n  DDR 1600-3200MB/s 2.5V 2n
    - DDR2 3.2-6.4GB/s 1.8V 4n  DDR3 6.4-16.8GB/s 1.5-1.35V 8n  DDR4 12.8-25.6GB/s 1.2V 8n

- Low power DRAMs, mainly 1-2/mobile appliance, 16 or 32b device width: *
  - LPSDR 533-667MB/s  LPDDR 800-1067MB/s 1.8V 2n  LPDDR2 3.2-4.3GB/s 1.2V 4n
  - LPDDR3 6.4-8.5GB/s 1.2V 8n  LPDDR4 12.8-17.1GB/s 1.1V 16n

- Graphics DRAMs, similar progression, most recent is GDDR5 family, 32b wide
  - Low end of 12.8GB/s 8n, High end of 56GB/s 8n/16n GDDR5X single chip

FPM – fast page mode, EDO – extended data out, S – single, D – double, DR – data rate, _n – prefetch
* Bandwidths shown for single 32b device
## High Performance DRAM Comparison

<table>
<thead>
<tr>
<th>Type</th>
<th>DDR3/DDR3L</th>
<th>DDR4</th>
<th>LPDDR4</th>
<th>GDDR5N</th>
<th>RL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Density</td>
<td>Up to 16Gb</td>
<td>Up to 16Gb</td>
<td>Up to 32Gb</td>
<td>Up to 8Gb</td>
<td>Up to 1Gb</td>
</tr>
<tr>
<td>Prefetch Size</td>
<td>8n</td>
<td>8n</td>
<td>16n</td>
<td>8n</td>
<td>2n</td>
</tr>
<tr>
<td>Core Voltage (Vdd)</td>
<td>1.5V/1.35V</td>
<td>1.2V</td>
<td>1.10</td>
<td>1.35V</td>
<td>1.35V</td>
</tr>
<tr>
<td>I/O Voltage</td>
<td>Same as VDD</td>
<td>Same as VDD</td>
<td>Same as VDD</td>
<td>Same as VDD</td>
<td>1.2V</td>
</tr>
<tr>
<td>Max Clock Frequency</td>
<td>1066MHz</td>
<td>1600MHz</td>
<td>2133MHz</td>
<td>1250MHz</td>
<td>1200MHz</td>
</tr>
<tr>
<td>Max Data Rate</td>
<td>DDR2100</td>
<td>DDR3200</td>
<td>DDR4267</td>
<td>DDR5000</td>
<td>DDR2400</td>
</tr>
<tr>
<td>Burst Length</td>
<td>BC4, 8</td>
<td>BC4, 8</td>
<td>16, 32</td>
<td>8</td>
<td>2,4,8</td>
</tr>
<tr>
<td>Device Width (I/O)</td>
<td>x4, x8, x16</td>
<td>x4, x8, x16</td>
<td>2Ch x16</td>
<td>x16,x32</td>
<td>x18, x36</td>
</tr>
<tr>
<td>Internal Banks</td>
<td>8</td>
<td>16 (x4/x8), 8 (x16)</td>
<td>8/Ch</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Bank Groups</td>
<td>N/A</td>
<td>4 (x4/x8), 2 (x16)</td>
<td>N/A</td>
<td>4</td>
<td>N/A</td>
</tr>
<tr>
<td>On Die Temperature Sensor</td>
<td>Optional/RS</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>N/A</td>
</tr>
<tr>
<td>Row Cycle Time (tRC)</td>
<td>43 to 52ns</td>
<td>45 to 50ns</td>
<td>60 to 63ns</td>
<td>40 to 44ns</td>
<td>6.67 to 8ns</td>
</tr>
<tr>
<td>Bank Address Delays</td>
<td>5.0–10ns/ 25–40ns</td>
<td>2.5–7.5ns/ 10–35ns</td>
<td>10ns/ 40ns</td>
<td>4ns/ 16ns</td>
<td>NA</td>
</tr>
<tr>
<td>(tRRD/tFAW)*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus Turn Delay (tWTR)*</td>
<td>7.5ns</td>
<td>2.5 to 11.25ns</td>
<td>10ns</td>
<td>5.1 to 5.6ns</td>
<td>0.83 to 1.07ns</td>
</tr>
<tr>
<td>Refresh Penalty (tRFC)</td>
<td>110-350ns</td>
<td>160-350ns</td>
<td>130-180 (all bank)</td>
<td>60-90 (per bank)</td>
<td>65-110ns</td>
</tr>
</tbody>
</table>

*Minimum associated clock cycles may also apply*
Very High Bandwidth Options

- Micron pioneered TSV-based DRAM, 2011 introduction of HMC gen1

- HMC gen2 in production, stack bandwidth tuned to SerDes technology
  - Hybrid Memory Cube: multiple layers of DRAM attached using TSV onto foundry process high performance logic layer, Processing At Memory Atomic operations
  - Complete high reliability module

- HBM2, JEDEC, 2Gb/s 1024b = 256GB/s peak (4 DRAMs, 1 redistribution die)
  - Means provided for some management of yield and errors but not comparable to HMC
  - Very complex manufacturing engagements

- GDDR5X, JEDEC, 14Gb/s 32b, for 4 die 224GB/s in only 128 data bits
  - Generally most economical way to achieve highest bandwidth/system

TSV – Through Silicon Via
HMC – Abstracted Memory Management

“Vaults” Versus Arrays

**Increased Bandwidth**
- 16 vaults correspond to 16 independent memory channels
- Internal memory bandwidth matches external link capability
- Host interface can send/receive continuous requests (gapless)

**Increased Quality and Reliability**
- Self test, error detection, correction, and repair within vaults controlled by Logic Base

Logic Base Controls Memory Functions

**Reduced Memory Complexity**
- DRAM controlled by HMC logic base, not host controller
- Host memory operations are simplified to requests and responses

**Increased Performance**
- Internal memory bandwidth matches external link capability
- Host interface can send/receive continuous requests (gapless)
HMC – Reliability and Utility

- Extraordinary Reliability, Availability and Serviceability (RAS) Features
- Scrubbing, Correction of soft errors, In-Field Repair of hard errors
- Error and Warning reporting through in-band or side-band options
- Strong link CRC protection and retry mechanism
  - Much higher correctness certainty than JEDEC adopted CRCs
- Packet integrity checked before operations
- Internal signals between logic layer and DRAM also protected
- Atomic operations for application acceleration
  - Observed 2-4x additional speedup beyond performance improvement from bandwidth
- Scale-out capability: device chaining, networks of HMCs, etc.
Memory / Storage Technology Hierarchy

Latency, not to scale

Nanoseconds

Memory Control
(Load/Store)

Performance Optimized PM

RDIMM/LRDIMM
(DRAM)

NVDIMM-N
(DRAM/NAND)

ASP/Bit

Cost Optimized PM

DIMMs
(3D XPoint™ memory)

Microseconds

I/O Control
(Read/Write)

NVME SSD
(NAND)

NVME SSD
(3D XPoint™ memory)

SATA/SAS SSD
(NAND)

Milliseconds

Hard Disk Drive
(Spinning Media)

Storage I/O
Memory
Persistent Memory

Hard Disk Drive

Latency, not to scale
Persistent Memory & NVDIMM

- NVDIMM - the persistent memory solution available TODAY

- Micron’s NVDIMM – delivers DRAM read and write performance with the persistence and reliability of NAND

- Combines NAND Flash, DRAM, and a power source into a memory subsystem

- Backs up DRAM data if power is interrupted
Developing New Markets

Relational Databases
- Microsoft® SQL
- MySQL™

Big Data Analytics
- HortonWorks®
- Cassandra™

Scale-out Storage
- VMware® VSAN
- Microsoft® Azure™

In-Memory Databases
- SAP® HANA
- Microsoft® SQL Hekaton

Trademarked software named to identify primary segment applications. Their use does not represent an endorsement of Micron or Micron NVDIMM products.
Case Studies: Real-World Results

Early block-mode results

- **2X+ faster database logging** performance for Microsoft® SQL Server

- Up to **4X+ faster SQL cluster replications** when moving the log from NAND flash to HPE NVDIMMs

- **2X+ faster transaction rates** in Linux® applications when using HPE NVDIMMs

- Up to **63% faster exchange speeds**

Source: [HPE public data sheets](#) and media interviews. HPE lab testing on a DL380 Gen9 Server with E5 2600 v4 processor and 8 GB HPE NVDIMM.

### MongoDB

- **6-9X latency improvement**

Source: [Plexistor public case study](#). Dual socket XEON E5-2650v3, enterprise SATA SSD, 64GB DDR4 DIMM vs. 64GB DDR4 NVDIMM-N
Future Mainstream Memory

- Future graphics and low power DRAM architectures in work

- DDR5 for ~2018 samples, ~2019 production, details subject to change
  - 8-32Gb capacity, 3.2-6.4Gbps IO, 1.1V, 16n prefetch, 16-32 banks in 8 groups
  - Basically 2x bandwidth of DDR4, some innovations at module level too

- All good, but...

- Most interesting is the new class of memory from Micron / Intel
A TIMELINE OF MEMORY CLASS INTRODUCTIONS

1947 Ram
1956 SRAM
1961 DRAM
1966 EPROM
1971 NOR Flash Memory
1984 NAND Flash Memory
1989 3D XPoint™ Memory
2015

IT’S BEEN DECADES SINCE THE LAST MAINSTREAM MEMORY
Nonvolatile Memories in Server Architectures

• 3D XPoint™ technology provides the benefit in the middle
• It is considerably faster than NAND Flash
• Performance can be realized on PCIe or DDR buses
• Lower cost per bit than DRAM while being considerably more dense
New Persistent Memory: 3D XPoint™ Technology

**Value Proposition**

- DRAM-like performance with higher density and lower standby energy
- Non-volatility with fraction of DRAM cost/bit
- Ideal for large memory systems such as in-memory-database/in-memory-compute/analytics

<table>
<thead>
<tr>
<th></th>
<th>NAND</th>
<th>3D XPoint</th>
<th>DRAM</th>
</tr>
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<tbody>
<tr>
<td><strong>Latency</strong></td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td><strong>Volatility</strong></td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td><strong>Relative Cost</strong></td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
</tbody>
</table>

3D XPoint™ Memory Wafer
Near-term System Concept

Host with Fast Near Memory

Multiple Processor Cores and Uncore

Near Memory DRAM

DRAM DIMMs

Working Memory

Bulk DRAM
~100ns latency (Load to Use)

Far Memory

ASICs and DRAM caching

3D XPoint™

Latency to be announced

Storage

ASICs and DRAM caching

3LC 3D NAND

SSD
> 50,000 ns best latency
Summary

- All memory continues to scale, increasingly difficult and complex
- New DRAM architectures in work across all major application areas
- Numerous very high bandwidth options with GDDR5X as highest BW/$
- HMC delivers unique advantages for ultra-high bandwidth applications
- Emergence of Persistent Memory, first as DRAM+NAND NVDIMM
  - Evolving, enabling new and better products
- 2016 production of first new memory technology in decades: 3D XPoint™ Memory
- The future: blending the many existing and new memory types
  - Overall cost and performance tuned to the application