A NEW X86 CORE ARCHITECTURE FOR THE NEXT GENERATION OF COMPUTING

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# AGENDA

## THE ROAD TO ZEN

### HIGH LEVEL ARCHITECTURE

- Improvements in Core Engine
- Floating Point
- Improvements in Cache System
- SMT Design to Maximize Throughput
- New ISA Extensions

## SUMMARY

## NEXT STEP UP
AMD X86 CORES: DRIVING COMPETITIVE PERFORMANCE

*Based on internal AMD estimates for “Zen” x86 CPU core compared to “Excavator” x86 CPU core.

More Instructions Per Clock*

40%
AMD CPU DESIGN OPTIMIZATION POINTS

ONE CORE FROM FANLESS NOTEBOOKS TO SUPERCOMPUTERS

“ZEN”

+40% Higher IPC*

Low Power “Jaguar”

High Performance “Excavator”

LOWER POWER  MORE PERFORMANCE
SMALLER  MORE AREA, POWER

*Based on internal AMD estimates for “Zen” x86 CPU core compared to “Excavator” x86 CPU core.
DEFYING CONVENTION: A WIDE, HIGH PERFORMANCE, EFFICIENT CORE

“ZEN”

Instructions-Per-Clock

Total Efficiency Gain

Energy Per Cycle

At = Energy Per Cycle

+40% work per cycle*

“Steamroller”

“Piledriver”

“Excavator”

“Bulldozer”

*Based on internal AMD estimates for “Zen” x86 CPU core compared to “Excavator” x86 CPU core.
ZEN PERFORMANCE & POWER IMPROVEMENTS

**BETTER CORE ENGINE**
- Two threads per core
- Branch mispredict improved
- Better branch prediction with 2 branches per BTB entry
- Large Op Cache
- Wider micro-op dispatch 6 vs. 4
- Larger Instruction Schedulers Integer: 84 vs. 48 | FP: 96 vs. 60
- Larger retire 8 ops vs. 4 ops
- Quad issue FPU
- Larger Retire Queue 192 vs. 128
- Larger Load Queue 72 vs. 44
- Larger Store Queue 44 vs. 32

**BETTER CACHE SYSTEM**
- Write back L1 cache
- Faster L2 cache
- Faster L3 cache
- Faster Load to FPU: 7 vs. 9 cycles
- Better L1 and L2 data prefetcher
- Close to 2x the L1 and L2 bandwidth
- Total L3 bandwidth up 5x

**LOWER POWER**
- Aggressive clock gating with multi-level regions
- Write back L1 cache
- Large Op Cache
- Stack Engine
- Move elimination
- Power focus from project inception
- Low Power Design Methodologies

40% IPC PERFORMANCE UPLIFT
**ZEN MICROARCHITECTURE**

- Fetch Four x86 instructions
- Op Cache instructions
- 4 Integer units
  - Large rename space – 168 Registers
  - 192 instructions in flight/8 wide retire
- 2 Load/Store units
  - 72 Out-of-Order Loads supported
- 2 Floating Point units x 128 FMACs
  - built as 4 pipes, 2 Fadd, 2 Fmul
- I-Cache 64K, 4-way
- D-Cache 32K, 8-way
- L2 Cache 512K, 8-way
- Large shared L3 cache
- 2 threads per core
Decoupled Branch Prediction

TLB in the BP pipe
- 8 entry L0 TLB, all page sizes
- 64 entry L1 TLB, all page sizes
- 512 entry L2 TLB, no 1G pages

2 branches per BTB entry

Large L1 / L2 BTB

32 entry return stack

Indirect Target Array (ITA)

64K, 4-way Instruction cache

Micro-tags for IC & Op cache

32 byte fetch
DECODE

- Inline Instruction-length Decoder
- Decode 4 x86 instructions
- Op cache
- Micro-op Queue
- Stack Engine
- Branch Fusion
- Memory File for Store to Load Forwarding
EXECUTE

- 6x14 entry Scheduling Queues
- 168 entry Physical Register File
- 6 issue per cycle
  - 4 ALU's, 2 AGU's
- 192 entry Retire Queue
- Differential Checkpoints
- 2 Branches per cycle
- Move Elimination
- 8-Wide Retire
LOAD/STORE AND L2

- 72 Out of Order Loads
- 44 entry Store Queue
- Split TLB/Data Pipe, store pipe
- 64 entry L1 TLB, all page sizes
- 1.5K entry L2 TLB, no 1G pages
- 32K, 8 way Data Cache
  - Supports two 128-bit accesses
- Optimized L1 and L2 Prefetchers
- 512K, private (2 threads), inclusive L2
- 2 Level Scheduling Queue
- 160 entry Physical Register File
- 8 Wide Retire
- 1 pipe for 1x128b store
- Accelerated Recovery on Flushes
- SSE, AVX1, AVX2, AES, SHA, and legacy mmx/x87 compliant
- 2 AES units
ZEN CACHE HIERARCHY

- Fast private 512K L2 cache
- Fast shared L3 cache
- High bandwidth enables prefetch improvements
- L3 is filled from L2 victims
- Fast cache-to-cache transfers
- Large Queues for Handling L1 and L2 misses
A CPU complex (CCX) is four cores connected to an L3 Cache.

- The L3 Cache is 16-way associative, 8MB, mostly exclusive of L2.
- The L3 Cache is made of 4 slices, by low-order address interleave.
- Every core can access every cache with same average latency.
**SMT OVERVIEW**

- All structures fully available in 1T mode
- Front End Queues are round robin with priority overrides
- Increased throughput from SMT

- **Competitively shared structures**
- **Competitively shared and SMT Tagged**
- **Competitively shared with Algorithmic Priority**
- **Statically Partitioned**
**NEW INSTRUCTIONS**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Notes</th>
<th>Excavator</th>
<th>Zen</th>
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</thead>
<tbody>
<tr>
<td>ADX</td>
<td>Extending multi-precision arithmetic support</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>RDSEED</td>
<td>Complement to RDRAND random number generation</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>SMAP</td>
<td>Supervisor Mode Access Prevention</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>SHA1/SHA256</td>
<td>Secure Hash Implementation Instructions</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CLFLUSHOPT</td>
<td>CLFLUSH ordered by SFENCE</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>XSAVEC/XSAVES/XRSTORS</td>
<td>New Compact and Supervisor Save/Restore</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>CLZERO</td>
<td>Clear Cache Line</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>PTE Coalescing</td>
<td>Combines 4K page tables into 32K page size</td>
<td></td>
<td>✓</td>
</tr>
</tbody>
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We support all the standard ISA including AVX & AVX-2, BMI1 & BMI2, AES, RDRAND, SMEP

*AMD Exclusive*
“ZEN”

Totally New High-performance Core Design

New High-Bandwidth, Low Latency Cache System

Simultaneous Multithreading (SMT) for High Throughput

Energy-efficient FinFET Design Scales from Enterprise to Client Products
A COMMITTED ROADMAP TO X86 PERFORMANCE

INSTRUCTIONS PER CLOCK

“Bulldozer” Core

“Excavator” Core

“ZEN”

40%

More Instructions Per Clock*

“ZEN+”

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