No Transistor Left Behind

By Raja Koduri
A tribute to
Frances Allen

“Who Helped Hardware Understand Software”
“No Transistor Left Behind”

DAVID BLYTHE, 2018
Technology Led Disruptions

PC ERA
1B Internet Connected Devices

Digitize Everything
Network Everything

Technology Led Disruptions

MOBILE + CLOUD ERA
10B Cloud Connected Devices

- Cloud Everything
- Mobile Everything
- Network Everything
- Digitize Everything
Technology Led Disruptions

- Digitize Everything
- Network Everything
- Mobile Everything
- Cloud Everything
- Exascale

100B Intelligent Connected Devices

For Everyone
Intelligence is Expensive

Alex-Net to AlphaGo Zero: 300,000x Increase in Compute

2-year doubling (Moore’s law)

3.4-month doubling

Source: AI and Compute • November 7, 2019 • Dario Amodei & Danny Hernandez
**Performance and Generality**

- **Performance**
  - Human level
  - Unconstrained world
    - General Purpose
  - Constrained world
    - Fixed function

- **Generality**
  - Human
  - Human level intelligence

- **Examples**
  - Humanoid robots
  - Machine translations
  - Image classification
  - Chess

*Graph: Illustrative purposes only

Rohrer, B., 2018. Getting Closer To Human Intelligence Through Robotics. [Youtube](https://www.youtube.com/watch?v=0ILdnZmp3lw&t=2095s)*
We are generating data at a faster rate than our ability to analyze, understand, transmit, secure and reconstruct in real-time.
Memory Wall

System Memory Bandwidth (TB/S)

Estimated Power (W)

5 – 10x power efficiency gap

AI MEM TARGET

Source: http://research.nvidia.com/publication/2017-02_architecting-an-energy-efficient
Data and Super Intelligence

- Human level
- Human
- Unconstrained world
- General Purpose
- Constrained world
- Fixed function
- Super Intelligence
- Generality
- Performance

- Humanoid robots
- Image classification
- Chess
- Machine translations


*Graph: Illustrative purposes only
"The biggest lesson that can be read from 70 years of AI research is that general methods that leverage computation are ultimately the most effective, and by a large margin. The ultimate reason for this is Moore's Law."

RICH SUTTON, THE BITTER LESSON, MARCH 2019
“The number of people predicting the death of Moore’s law doubles every two years”
“Everything that can be invented has been invented”
Charles H. Duell - US Patent Commissioner 1899

“Moore’s law won’t work at feature sizes less than a quarter of a micron”
Erich Bloch – Head of IBM Research, later Chairman of NSF 1988

Moore Sees ‘Moore’s Law’ Dead in a Decade
By Mark Hatchman on September 18, 2007 at 5:12 pm | 1 Comment
2007

In a “fireside chat” with NPR’s “Tech Nation’s” Moira Gunn, Intel co-founder and chairman emeritus Gordon Moore said he sees his famous law expiring in 10 to 15 years.

Theoretical physicist: Moore's Law has just 10 years to go
The age of silicon will come to a close but nobody knows when. Well, almost nobody. 2012

Report: IBM researcher says Moore's Law at end
IBM Fellow Carl Anderson says at a conference this week that Moore’s Law is hitting a ceiling, according to a report. 2009

Moore’s Law limit hit by 2014?
The high cost of semiconductor manufacturing equipment is making continued chipmaking advancements too expensive, threatening Moore’s Law, according to iSuppli. 2009

Moore’s Law Is Dead. Now What?
Shrinking transistors have powered 50 years of advances in computing — but now other ways must be found to make computers more capable. 2016

“There is nothing new to be discovered in physics now”
Lord Kelvin 1900

Death of Moore’s Law Will Cause Economic Crisis
“Around 2020 or soon afterward, Moore’s law will gradually cease to hold true and Silicon Valley may slowly turn into a rust belt unless a replacement technology is found,” says Kaku in an extract published on Salon.com website. 2011

The End of Moore's Law?
The current economic boom is likely due to increases in computing speed and decreases in price. Now there are some good reasons to think that the party may be ending.

by Charles C. Mann 2000
Moore’s Law - Our Exponential Entitlement

Based on Intel Internal Data
... we haven’t fully exploited what was given to us by Moore!
Software Productivity vs. Hardware Efficiency

for i in xrange(4096):
    for j in xrange(4096):
        for k in xrange(4096):
            C[i][j] += A[i][k] * B[k][j]
Training & Inference Software Speed-Up

On Intel Xeon

“What Andy Giveth, Bill Taketh Away”
"There's still plenty of room at the bottom"
"There's still plenty of room at the bottom"

A path to 50x Transistor Density
FinFET

Intel 10nm

NMOS

PMOS
Intel 10nm

FinFET

Pitch Scaling

NMOS

PMOS

Density Increase

TOTAL

x3
Pitch Scaling

Nanowire

Density Increase

$\times 2$

Total

$\times 6$
Nanowire Stack

NMOS  PMOS

Stacked Nanowire

Density Increase

x2

Total

x12
Wafer to Wafer Stacking
Die to Wafer Stacking

DENSITY INCREASE
x2
TOTAL
~x50
What about Power?

Innovations

- Base Line
- Voltage Scaling
- Capacitance Scaling
- New Packaging
- Frequency Scaling
- New Architectures

50x

For illustrative purposes only
Case for Advanced Packaging

**Transistor Design Target Range**

- Desktop CPU
- High Perf FPGA
- Server CPU
- dGPU
- Mobile CPU
- Power Efficient FPGA
- iGPU
- Entry CPU/PCH

**Transistor Diversity**

- Logic Transistors
- Analog/RF Transistors
- High Speed Memory
- Dense Memory
- Non-Volatile Memory
- High speed IO
- Configuration Memory

No single transistor node is optimal across all design points!
Packaging Technology Improvements

- **2D / 2.5D**
  - BUMP PITCH: 100 um
  - BUMP DENSITY: 100/mm²
  - POWER: 1.7 pJ/bit

- **3D**
  - BUMP PITCH: 50 – 25 um
  - BUMP DENSITY: 400-1,600/mm²
  - POWER: 0.15 pJ/bit

- **FUTURE**
  - BUMP PITCH: < 10 microns
  - BUMP DENSITY: > 10,000/mm²
  - POWER: < 0.05 pJ/bit

Interconnect Density vs. Power Efficiency chart.
Hybrid Bonding

Dense vertical interconnects

- Smaller, simpler circuits
- Lower capacitance
- Lower power

Area scales with bump pitch

50 um Pitch
Lakefield
400 bumps/mm²

10 um Pitch
Hybrid Bonding
10000 bumps/mm²
Advanced Packaging Products

**KABY LAKE G**
2D
- Intel CPU
- AMD GFX
- HBM

**LAKEFIELD**
3D
- Internal Silicon on Multiple Nodes

**AGILEX FPGA**
2.5D
- Intel FPGA
- Foundry IO Chiplets
- HBM

**PONTE VECCHIO**
3D
- Internal and External Silicon on Multiple Nodes
Memory Wall

Source: http://research.nvidia.com/publication/2017-02_architecting-an-energy-efficient
Memory Hierarchy Disruptions

- **COMPUTE CACHE**: 100s MB, ~1ns
- **IN-PACKAGE MEMORY**: 1s GB, ~10ns
- **MEMORY**: 10s GB, <100ns
- **SECONDARY STORAGE**: 100s GB, <1sec
- **TERTIARY STORAGE**: 1s TB, <10µsecs
- **STORAGE PERFORMANCE GAP**: 10s TB, <100µsecs
- **COST-PERFORMANCE GAP**: 10s TB, <10 msecs

Memory

- **CAPACITY GAP**: 10s GB, <100ns

Storage
Memory Hierarchy Disruptions

- **Compute Cache**: 100s MB, ~1ns
- **In-Package Memory**: 1s GB, ~10ns
- **Memory**: 10s GB, <100ns
- **Persistent Memory**: 100s GB, <1sec
- **3D XPoint**: 1s TB, <10μsecs
- **3D QLC NAND**: 10s TB, <100μsecs
- **Tertiary Storage**: 10s TB, <10msecs

**Memory**: Capacity Gap

**Storage**: Storage Performance

- **Capacitance**: Memory storage with 10s GB, <100ns
- **Storage**: Secondary storage with 10s TB, <10μsecs
- **Tertiary Storage**: Tertiary storage with 10s TB, <10msecs
Compute and Memory

a Vision for Next Gen

- 10x on capacity
- 10x more B/W
- 10x lower latency
- 10x lower power

- 10s MB, ~1ns
- 1s GB, ~10ns
- 10s GB, <100ns
- 10s TB, <100μsecs
- 10s TB, <10 ms
Compute and Memory

a Vision for Next Gen

NEW MEMORY?

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<tr>
<td>CAPACITY</td>
<td>10 – 100s GB</td>
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<tr>
<td>LATENCY</td>
<td>&lt; 10ns</td>
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TIGHTLY INTEGRATED WITH COMPUTE
“Plenty of Room at the Bottom”

“What would happen if we could arrange atoms one by one the way we want them?”

“When we get to circuits of, say 7 atoms – we will have new opportunities for design. We will manufacture in different ways”

RICHARD FEYNMAN, 1959
Beyond Exascale Compute
General Flow of Architecture
In Hardware Companies

1st STEP
WHITEBOARD

2nd STEP
SPREADSHEET

3rd STEP
SIMULATOR

MAKE IT REAL
1 Core
SINGLE DIE

~25

TOTAL # OF CORES
25

1 Core
PACKAGE
x2
TOTAL # OF CORES
50

1 Core
1 Core

DENSITY.scaling

x50

TOTAL # OF CORES
2500
PACKAGE PER BOARD

x4

TOTAL # OF CORES
10,000

1 Core
“Software is Eating the World”

MARC ANDREESSEN, 2011
Compute Disruptions

PC ERA
>1M PC DEVELOPERS

Digitize Everything

X86 + Windows

Network Everything

Compute Disruptions

MOBILE + CLOUD ERA
>10M MOBILE + CLOUD DEVELOPERS
+ x86

Cloud Everything

Mobile Everything

Network Everything

Digitize Everything

Architecture Impact

PERFORMANCE X GENERALITY
>20M
Developers

x86 Developer Ecosystem

DEVELOPER TOOLS

SERVICES & SOLUTIONS

APPLICATIONS

MIDDLEWARE FRAMEWORKS AND RUNTIMES

LOW LEVEL LIBRARIES

VIRTUALIZATION/ ORCHESTRATION

OS

DRIVERS

FW IP & BIOS

x86

Developers
Software Stack & Developers

- Driven by Abstraction
  - Services & Solutions
  - Applications
  - Middleware Frameworks and Runtimes
  - Low Level Libraries
  - Virtualization/Orchestration
  - OS
  - Drivers
  - FW IP & BIOS
  - x86

- Affinity to Hardware

# of Developers:
- 20M
- 500K
- 50K
# Stack and Swiss Cheese

Middle is full of "holes"
New Hardware / Software Contracts

The Reality...

“IT JUST WORKS”

“IT ALMOST WORKS”

New Hardware/Software Contract
What is the Hardware / Software Contract for the next Era?

**PC ERA**
>1M PC DEVELOPERS

- X86 + Windows

**Digitize Everything**

**Mobile Everything**

**Network Everything**

**MOBILE + CLOUD ERA**
>10M MOBILE + CLOUD DEVELOPERS  
+ PC DEVELOPERS

- Apple
- Android
- arm

- x86

**Cloud Everything**

**INTELLIGENCE ERA**
>100M  
+ AI DEVELOPERS
+ MOBILE + CLOUD DEVELOPERS  
+ PC DEVELOPERS

**Intelligent Everything**

- x86
- arm
- RISC-V
- AI
- GPU
- MEMORY
- NETWORK

Intel

Generality $\propto \frac{1}{\text{Architecture Heterogeneity}}$
Heterogeneous Math in CPU

For illustrative purposes only
Heterogeneous Math in CPU

For illustrative purposes only
CPU Impact with ISA Extensions & Software

- Generality
- HETERO EXTENSIONS
- Gap Covered by Software
  Increasing Impact

Performance

CPU CORE
CPU Impact with ISA Extensions & Software

~3-5 YEARS TO REACH BROAD ADOPTION
Productivity and Scale

Mandelbrot Static Instructions Generated per Line of Code

For illustrative purposes only
ABSTRACTION REQUIREMENTS

SCALABLE AND OPEN
ABSTRACTION REQUIREMENTS

SCALABLE AND OPEN

ABSTRACT AT MULTIPLE LAYERS
Performance vs. Productivity
Mandelbrot Static Instructions Generated per Line of Code

For illustrative purposes only
ABSTRACTION REQUIREMENTS

SCALABLE AND OPEN

ABSTRACT AT MULTIPLE LAYERS

SUPPORT NINJA'S ACROSS THE ENTIRE STACK
Generality $\propto 1$/ Architecture Heterogeneity

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Abstraction Required at Multiple Layers
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- **CPU**
- **GPU**
- **AI**
- **FPGA**
- **INTERCONNECT**
- **MEMORY**
# oneAPI Abstraction Roadmap

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**oneAPI**

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Hardware / Software Contract Layer

- **Software**
- **Hardware**

**SCALABLE HARDWARE ABSTRACTION LAYER**

- **LEVEL ONE**
  - MIDDLEWARE FRAMEWORKS AND RUNTIMES
  - LOW LEVEL LIBRARIES
- **LEVEL ZERO**
  - VIRTUALIZATION/ ORCHESTRATION
  - OS
  - DRIVERS
- **LEVEL SUBZERO**
  - FW IP & BIOS
  - CPU
  - GPU
  - AI
  - FPGA
  - INTERCONNECT
  - MEMORY
Goal of new HW/SW Contract

No Transistor Left Behind
From Sensors to Supercomputers - 2021

SENSORS

EDGE

DATA CENTER

SINGLE SOFTWARE ABSTRACTION

<1M NEURONS

TERA FLOPS

PETA FLOPS

EXA FLOPS

mWatts

Watts

kWatts

MWatts
From Sensors to Supercomputers - 2025

SENSORS

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From Sensors to Supercomputers - 2025

SENSEORS

EDGE

DATA CENTER

SINGLE SOFTWARE ABSTRATION

> 1B NEURONS

PETA FLOPS  EXA FLOPS  ZETTA FLOPS

EXAFLOPS ON THE EDGE ENABLE EXASCALE FOR EVERYONE
Summary

PERFORMANCE

PLENTY OF ROOM AT THE TOP

1000x

BY 2025

GENERALITY

PLENTY OF ROOM AT THE BOTTOM
“Optimism is the essential ingredient of innovation”

ROBERT NOYCE
THANK YOU

AND REMEMBER, LEAVE NO TRANSISTOR BEHIND
Legal Disclaimers

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