The Xe GPU Architecture

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The Road to X<sup>e</sup>

Gen 11  Gen 9  Gen 8  Gen 7  Gen 6  Gen 5  Gen 4  Gen 3  Gen 2  Gen 1

Discrete  Chipset  Integrated
Architecture Goals

SCALABILITY & CONFIGURABILITY

NEW CAPABILITIES

POWER, PERFORMANCE & AREA
Intel GPU Architecture
One Architecture and 4 Micro Architectures
- 3D / Compute Slice
- Media Slice
- Memory Fabric / Cache
3D/Compute Slice

- Variable number of Subslices
- 3D Fixed Function (optional)
  - Geometry
  - Setup and Raster
  - Color, Z, HiZ
**Xe Subslice**

- 16 EUs
- Thread dispatch
- Instruction cache
- L1, texture cache and shared local memory
- Load / Store
- Fixed Function (optional)
  - 3D sampler
  - Media sampler
  - Ray Tracing
Execution Unit

- Thread control
- Register file
- Branch
- Send
- Multiple issue ports
- Configurable mapping of vector pipes
  - Floating Point
  - Integer
  - Extended Math
  - FP64 (optional)
  - Matrix Extension (XMX) (optional)
Media Slice

- Media slices are independent
- Software can distribute a high-resolution stream across multiple slices
- Fixed function units:
  - MFX - encode / decode / transcode
  - SFC - scaling and format conversion
  - VQE - video quality engine
Memory Fabric

Coherent Scalable Interconnect Fabric

- Slices
- L3 + Rambo (optional)
- SoC infrastructure
  - PCIe
  - Display (optional)
  - Memory Controller
    - Local Memory (optional)
- Extendable (optional)
Intra-Package Scaling

- $X^e$ instantiated as a tile
- EMIB bridges interconnect tiles over $X^e$MF
- Package-time option to integrate up to 4 tiles
Inter-Package Scaling

- $X^e$ Link for system level scalability
- Connect through $X^e$MF
- $X^e_{\text{HPC}}$ implementation: I/O tiles and EMIB
## Micro-architectures

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<td>Tiger Lake</td>
<td>DG1</td>
<td>SG1</td>
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<td><strong>Discrete Gaming Optimized</strong></td>
<td>Single slice design</td>
<td>GDDR6 memory</td>
<td>Ray tracing</td>
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<tr>
<td><strong>Machine Learning &amp; Media Optimized</strong></td>
<td>1-4 tiles per package</td>
<td>HBM2e memory</td>
<td>Xe Link interconnect</td>
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<tr>
<td><strong>HPC &amp; Machine Learning Optimized</strong></td>
<td>1-2 tiles per package</td>
<td>HBM2e memory</td>
<td>Co-EMIB (Foveros + EMIB)</td>
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- Xe LP: Low Power Optimized
- Xe HPG: Discrete Gaming Optimized
- Xe HP: Machine Learning & Media Optimized
- Xe HPC: HPC & Machine Learning Optimized

**In production:**
- **Tiger Lake**
- DG1
- SG1

**In the lab:**
- TBD

**In fabrication:**
- TBD
- Ponte Vecchio
Ambitious Goals

~2X 3D/Compute performance at ~iso-area and ~iso-power vs. prior generation

Tiger Lake SoC with $X^e_{LP}$ GPU
$X_e^{LP}$ 1.5x Larger Engine

- Up to 96 EUs
- 1536 Flops/Clock
- Up to 48 Texels/Clock
- Up to 24 Pixels/Clock
Efficiency Improvements

- Frequency uplift at iso voltage
- Greater dynamic range
- Repipelining
- Bottlenecks analysis
Execution Unit

- High-efficiency thread control
  - Software scoreboarding
  - Pairs of EUs run in lockstep
- 8-wide FP/INT ALU
  - 2x INT16 and INT32 rates
  - Fast INT8 with DP4A
- 2-wide Extended Math ALU
Memory System

- New L1 data cache
- Up to 16 MB L3
- 2x GTI bandwidth
- End-to-end compression
- Support for local memory (optional)
Media Engine

- Up to 2x encode/decode throughput
- AV1 decode acceleration
- HEVC screen content coding support
- 4K/8K60 playback
- HDR/Dolby Vision playback
- 12-bit end-to-end video pipeline
**Multi-tile GPU**

1-Tile
>10 FP32 TFLOPS

2-Tile
>20 FP32 TFLOPS

4-Tile
>40 FP32 TFLOPS
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<td>HPC</td>
<td>COMPUTE TILE</td>
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Recap

Highly Configurable as family of microarchitectures

Scalable to 1000s of Execution Units

New Capabilities across 3D, Compute, Media, Display

Significant Perf/W and Perf/mm2 increases
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