IBM’s POWER10 Processor

Hot Chips 32
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IBM POWER Processor Technology Roadmap

POWER7/7+
- 45/32 nm
- Multi-core Optimized
- Up to 8 cores/die (32 HW threads)
- eDRAM L3 Cache
- Up to 8 cores/die
- Agnostic Memory
- Enterprise Focus
- Big Data Optimized
- PCIe G3 / CAPI / NVLINK
- OpenPOWER

POWER8 Family
- 22nm
- Agnostic Memory
- Enterprise Focus
- Big Data Optimized
- PCIe G3 / CAPI / NVLINK

POWER9 Family
- 14nm
- Up to 12 cores/die
- (96 HW threads)
- Modular new Core uArch
- Direct-Attach Memory
- OMI Memory
- PowerAXON Modular Attach
- PCIe G4 / CAPI 2.0
- Coherent NVLINK / OpenCAPI
- #1, #2 Supercomputers

POWER10 Family
- 7nm
- Up to 24/12 cores/die
- (96 HW threads)
- Modular Building Block Die
- New Core uArch
- AI-optimized ISA
- Energy Efficiency Focus
- HW Enforced Security
- Enterprise Focus
- PowerAXON 2.0
- PCIe G5
- Memory Clustering

POWER11 Family
- Under development...
- Up to 60/30 cores/socket (240 HW threads)
- Modular Building Block Die
- New Core uArch
- AI-optimized ISA
- Energy Efficiency Focus
- HW Enforced Security
- Enterprise Focus
- PowerAXON 2.0
- PCIe G5
- Memory Clustering

→ OpenPOWER
IBM POWER Processor Technology Roadmap: Today’s Discussion

POWER10 Family
7nm

Up to 60/30 cores/socket
(240 HW threads)
Modular Building Block Die
New Core uArch
AI-optimized ISA
Energy Efficiency Focus
HW Enforced Security
Enterprise Focus
PowerAXON 2.0
PCIe G5
Memory Clustering
POWER10 Design Focus

Data Plane Bandwidth, Capacity, Composability, Scale
Terabyte/second sockets, Petabyte system memory capacities, 16-socket SMP → Clusters

Powerful Enterprise Core
New Core Architecture, Flexibility, Larger caches, Reduced Latencies

End-to-end Security
Hardware enabled and co-optimized with PowerVM hypervisor

Energy Efficiency
3x improvement over POWER9

AI-Infused Core
10-20x matrix-math performance / socket compared to POWER9
POWER10 Processor Chip

**Technology and Packaging:**
- 602mm² 7nm Samsung (18B devices)
- 18 layer metal stack, enhanced device
- Single-chip or Dual-chip sockets

**Computational Capabilities:**
- Up to 15 SMT8 Cores (2 MB L2 Cache / core)
  (Up to 120 simultaneous hardware threads)
- Up to 120 MB L3 cache (low latency NUCA mgmt)
- 3x energy efficiency relative to POWER9
- Enterprise thread strength optimizations
- AI and security focused ISA additions
- 2x general, 4x matrix SIMD relative to POWER9
- EA-tagged L1 cache, 4x MMU relative to POWER9

**Open Memory Interface:**
- 16 x8 at up to 32 GT/s (1 TB/s)
- Technology agnostic support: near/main/storage tiers
- Minimal (< 10ns latency) add vs DDR direct attach

**PowerAXON Interface:**
- 16 x8 at up to 32 GT/s (1 TB/s)
- SMP interconnect for up to 16 sockets
- OpenCAPI attach for memory, accelerators, I/O
- Integrated clustering (memory semantics)

**PCIe Gen 5 Interface:**
- x64 / DCM at up to 32 GT/s

Die Photo courtesy of Samsung Foundry
Socket Composability: SCM & DCM

Single-Chip Module Focus:
- 602mm² 7nm (18B devices)
- Core/thread Strength
  - Up to 15 SMT8 Cores (4+ GHz)
- Capacity & Bandwidth / Compute
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x128 @ 32 GT/s
  - I/O: x32 PCIe G5
- System Scale (Broad Range)
  - 1 to 16 sockets

Dual-Chip Module Focus:
- 1204mm² 7nm (36B devices)
- Throughput / Socket
  - Up to 30 SMT8 Cores (3.5+ GHz)
- Compute & I/O Density
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x192 @ 32 GT/s
  - I/O: x64 PCIe G5
  - 1 to 4 sockets

(Multi-socket configurations show processor capability only, and do not imply system product offerings)
System Composability: **PowerAXON & Open Memory Interfaces**

- **PowerAXON & OMI Memory Interfaces**
- **Multi-protocol**
- **“Swiss-army-knife”**
- Flexible / Modular Interfaces

**POWER10 Chip**

- 1 Terabyte / Sec
- PowerAXON
- OMI Memory

**PowerAXON corner**
- 4x8 @ 32 GT/s

**OMI edge**
- 8x8 @ 32 GT/s

- **Built on best-of-breed**
- Low Power, Low Latency, High Bandwidth
- Signaling Technology

6x bandwidth / mm² compared to DDR4 signaling

IBM POWER10
System Enterprise Scale and Bandwidth: **SMP & Main Memory**

**Multi-protocol**
“Swiss-army-knife”
Flexible / Modular Interfaces

Allocate the bandwidth however you need to use it

Build up to 16 SCM socket
Robustly Scalable
High Bisection Bandwidth
“Glueless” SMP

Built on best-of-breed
Low Power, Low Latency,
High Bandwidth
Signaling Technology

1 Terabyte / Sec

POWER10 Chip

OMI Memory

Main tier DRAM

POWER10

1 Terabyte / Sec

SMP Interconnect

**Initial Offering:**
Up to 4 TB / socket
OMI DRAM memory
410 GB/s peak bandwidth
(MicroChip DDR4 buffer)
< 10ns latency adder

**DIMM swap upgradeable:**
DDR5 OMI DRAM memory with higher bandwidth and higher capacity

Allocate the bandwidth however you need to use it

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(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
Data Plane Bandwidth and Capacity: Open Memory Interfaces

OMI-attached GDDR DIMMs can provide low-capacity, high bandwidth alternative to HBM, without packaging rigidity & cost (Up to 800 GB/s sustained)

OMI-attached storage class memory can provide high-capacity, encrypted, persistent memory in a DIMM slot. (POWER10 systems can support 2 petabytes of addressable load/store memory)

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
System Heterogeneity and Data Plane Capacity: **OpenCAPI**

OpenCAPI attaches FPGA or ASIC-based Accelerators to POWER10 host with High Bandwidth and Low Latency.

OpenCAPI-attached storage class memory can provide high-capacity, encrypted, persistent memory in a device form factor. (POWER10 systems can support 2 petabytes of addressable load/store memory)

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
Pod Composability: PowerAXON Memory Clustering

Memory Inception capability enables a system to map another system’s memory as its own. Multiple systems can be clustered, sharing each other's memory.

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
Use case: Share load/store memory amongst directly connected neighbors within Pod
Unlike other schemes, memory can be used:
- As low latency local memory
- As NUMA latency remote memory

Example: Pod = 8 systems each with 8TB
Workload A Rqmt: 4 TB low latency
Workload B Rqmt: 24 TB relaxed latency
Workload C Rqmt: 8 TB low latency plus 16TB relaxed latency

All Rqmts met by configuration shown

POWER10 2 Petabyte memory size enables much larger configurations

(Memory cluster configurations show processor capability only, and do not imply system product offerings)
Memory Clustering: Enterprise-Scale Memory Sharing

Pod of Large Enterprise Systems
Distributed Sharing at Petabyte Scale

Or Hub-and-spoke with memory server
and memory-less compute nodes

(Memory cluster configurations show processor capability only, and do not imply system product offerings)
Memory Clustering: **Pod-level Clustering**

Use case: Low latency, high bandwidth messaging scaling to 1000’s of nodes

Leverage 2 Petabyte addressability to create memory window into each destination for messaging mailboxes

(Memory cluster configurations show processor capability only, and do not imply system product offerings)
IBM POWER10

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
POWER10 General Purpose Socket Performance Gains

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)
Powerful Core = Enterprise Strength + AI Infused

New Enterprise Micro-architecture
- Flexibility
  - Up to 8 threads per core / 240 per socket
- Optimized for performance and efficiency
  - +30% avg. core performance*
  - +20% avg. single thread performance*
  - 2.6x core performance efficiency* (3x @ socket)

AI Infused
- 4x matrix SIMD acceleration*
- 2x bandwidth & general SIMD*
- 4x L2 cache capacity with improved thread isolation*
- New ISA with AI data-types

1-2 POWER10 chips per socket
- Up to 30 SMT8 Cores
- Up to 60 SMT4 Cores

* versus POWER9

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)
Powerful Core : Enterprise Flexibility

Multiple World-class Software Stacks

Resilience and full stack integrity
- PowerVM, KVM
- AIX, IBMi, Linux on Power, OpenShift

Partition flexibility and security
- Full-core level LPAR
- Thread-based LPAR scheduling
- NEW: With PowerVM Hypervisor
  - Nested KVM + PowerVM
  - Hardware assisted container/VM isolation
## Powerful Architecture: AI Infused and Future Ready

**POWER10 implements Power ISA v3.1**

- v3.1 was the latest open Power ISA contributed to the OpenPOWER Foundation: Royalty free and inclusive of patents for compliant designs

### POWER10 Architecture – Feature Highlights

<table>
<thead>
<tr>
<th><strong>Prefix Architecture</strong></th>
<th>Greatly expanded opcode space, pc-relative addressing, MMA masking, etc.</th>
<th>RISC friendly 8B instructions including modified and new opcode forms.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>New Instructions and Datatypes</strong></td>
<td>New Scalar instructions for control flow, and operation symmetry</td>
<td>Set Boolean extensions; quad-precision extensions; 128b integer extensions; test LSB by byte; byte reverse GPR; int mul/div modulo; string isolate/clear; pause, wait-reserve.</td>
</tr>
<tr>
<td></td>
<td>New SIMD instructions for AI, throughput and data manipulation</td>
<td>32-byte load/store vector-pair; MMA (matrix math assist) with reduced precision; bfloat-16 converts; permute variations: extract, insert, splat, blend; compress/expand assist; mask generation; bit manipulation.</td>
</tr>
<tr>
<td><strong>Advanced System Features and Ease of Use</strong></td>
<td>Storage management</td>
<td>Persistent memory barrier / flush; store sync; translation extensions.</td>
</tr>
<tr>
<td></td>
<td>Debug</td>
<td>PMU sampling, filtering; debug watchpoints; tracing.</td>
</tr>
<tr>
<td></td>
<td>Hot/Cold page tracking</td>
<td>Recording for memory management.</td>
</tr>
<tr>
<td></td>
<td>Copy/Paste extensions</td>
<td>Memory movement; continued on-chip acceleration: Gzip, 842 compression, AES/SHA.</td>
</tr>
<tr>
<td><strong>Advanced EnergyScale</strong></td>
<td>Adaptive power management</td>
<td>Additional performance boost across the operating range.</td>
</tr>
<tr>
<td><strong>Security for Cloud</strong></td>
<td>Transparent isolation and security for enterprise cloud workloads</td>
<td>Nested virtualization with KVM on PowerVM; secure containers; main memory encryption; dynamic execution control; secure PMU.</td>
</tr>
</tbody>
</table>
**Security: End-to-End for the Enterprise Cloud**

### Crypto Performance:
- Core crypto improvements for today's algorithms (AES, SHA3) and ready for the future (PQC, FHE)

### Dynamic Execution Control Register (DEXCR)
- Performance enhanced side channel avoidance
- Main memory encryption: Stronger confidentiality against physical attacks
- Nested Virtualization – KVM on PowerVM:
  - Stronger container isolation without performance penalty
  - HW enabled and transparent
- Hardened container memory isolation

### Secure Containers:
- Transparent to applications
- End-to-end encryption

### Confidential Computing:
- • Transparent to applications
- • End-to-end encryption

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**IBM POWER10**
Powerful Core: Enterprise Strength

P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent

Fetch / Branch Predictors

L1 Instr. Cache
48k 6-way
<EA Tagged>

Instruction Buffer
128 entries

Decode/Fuse 8 iop

Instruction Table
512 entries

MMA Accelerator
2x512b

Execution Slice
128b

Execution Slice
128b

Execution Slice
128b

Execution Slice
128b

Load Queue
128 entries (SMT) 64 entries (ST)

Load Miss Queue
12 entries

Prefetch
16 streams

L1 Data Cache
32k 8-way
<EA Tagged>

Store Queue
80 entries (SMT) 40 entries (ST)

Store Queue
80 entries (SMT)

32B LD

32B LD

32B ST
(+gathered)

L2 Cache
(hashed index)

L3 Prefetch
48 entries

I miss

miss

ERAT
64 entry

TLB
4k entry

TLB miss

L3 prefetch

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Capacity vs. POWER9: Improved

>= 2x

= 4x
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA

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P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent

Fetch / Branch Predictors
- L1 Instr. Cache
  - 48k 6-way <EA Tagged>
  - 8 instr
- Instruction Buffer
  - 128 entries

Instruction Table
- 512 entries

MMA Accelerator
- 2x512b

Execution Slice
- 128b

L1 Data Cache
- 32k 8-way <EA Tagged>

Load Queue
- 128 entries (SMT)
- 64 entries (ST)

Load Miss Queue
- 12 entries

Prefetch
- 16 streams

2 Load EA

2 Store EA

ERAT
- 64 entry

L2 Cache
- (hashed index)

L1 Prefetch
- 48 entries

Store Queue
- 80 entries (SMT)
- 40 entries (ST)

Store Queue
- 80 entries (SMT)
- 40 entries (ST)

TLB miss

TLB
- 4k entry

L3 Prefetch
- 48 entries

Capacity vs. POWER9:
- Improved
- >= 2x
- = 4x
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
- Larger working-sets
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB

IBM POWER10

P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent

- Fetch / Branch Predictors
  - L1 Instr. Cache: 48k 6-way <EA Tagged>
  - Instruction Buffer: 128 entries
  - Decode/Fuse 8 iop
  - Execution Slice: 128b
  - MMA Accelerator: 2x512b
  - Load Queue: 128 entries (SMT) 64 entries (ST)
  - Load Miss Queue: 12 entries
  - Prefetch: 16 streams
  - Instruction Table: 512 entries
  - Execution Slice: 128b
  - L2 Cache (hashed index)
  - L1 Data Cache: 32k 8-way <EA Tagged>
  - Store Queue: 80 entries (SMT) 40 entries (ST)
  - Store Queue: 80 entries (ST) (+gathered)
  - TLB: 64 entry
  - TLB: 4k entry
  - L2 Cache: 64B dedicated
  - L3 Prefetch: 48 entries
  - Capacity vs. POWER9: Improved
  - >= 2x
  - = 4x
  - IBM POWER10
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
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- Deeper/wider instruction windows

P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
- Larger working-sets
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
- Deeper/wider instruction windows
- Data latency (cycles)
  - L2 13.5 (minus 2), L3 27.5 (minus 8)
  - L1-D cache 4 +0 for Store forward (minus 2)
  - TLB access +8.5 (minus 7)

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P10 Core Micro-architecture
½ SMT8 Core Resources Shown = SMT4 Core Equivalent

- Fetch / Branch Predictors
- L1 Instr. Cache 48k 6-way <EA Tagged>
- Instruction Buffer 128 entries
- Instruction Table 512 entries
- Execution Slice 128b
- MMA Accelerator 2x512b
- Load Queue 128 entries (SMT) 64 entries (ST)
- Load Miss Queue 12 entries
- Prefetch 16 streams
- L1 Data Cache 32k 8-way <EA Tagged>
- Store Queue 80 entries (SMT) 40 entries (ST)
- ERAT 64 entry
- TLB 4k entry
- L2 Cache (hashed index)
- L3 Prefetch 48 entries
- Predecode +Fusion/Prefix

Capacity vs. POWER9:
- Improved
- >= 2x
- = 4x
Powerful Core: Enterprise Strength

- Double SIMD + Inference acceleration
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  - TLB access +8.5 (minus 7)
- Branch
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT
Powerful Core: Enterprise Strength

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
- **Larger working-sets**
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
- **Deeper/wider instruction windows**
- **Data latency (cycles)**
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- **Branch**
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- **Fusion**
  - Fixed, SIMD, other: merge and back to back
  - Load, store: consecutive storage

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**P10 Core Micro-architecture**

1/2 SMT8 Core Resources Shown = SMT4 Core Equivalent

- **Fetch / Branch Predictors**
- **Instruction Table** 512 entries
- **MMA Accelerator** 2x512b
- **Load Queue** 128 entries (SMT) 64 entries (ST)
- **Load Miss Queue** 12 entries
- **Prefetch** 16 streams
- **Instruction Buffer** 128 entries
- **Decode/Fuse** 8 iop
- **L1 Instr. Cache** 48k 6-way <EA Tagged>
- **Instruction Table** 512 entries
- **Execution Slice** +Fuse 128b
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- **L1 Data Cache** 32k 8-way <EA Tagged>
- **Store Queue** 80 entries (SMT) 40 entries (ST)
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- **ERAT** 64 entry
- **TLB** 4k entry
- **L2 Cache** (hashed index)
- **L3 Prefetch** 48 entries

**Capacity vs. POWER9:**
- Improved
- >= 2x
- = 4x

IBM POWER10
**Powerful Core:** Energy Efficient

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
- Larger working-sets
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
- Deeper/wider instruction windows
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- Branch
  - Target registers with GPR in main regfile
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- Fusion
  - Fixed, SIMD, other: merge and back to back
  - Load, store : consecutive storage

- Improved clock-gating
- Design & micro-arch efficiency

![IBM POWER10 Block Diagram](image-url)

**Watt vs. POWER9:** Improved
Powerful Core: Energy Efficient

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
- **Larger working-sets**
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
- **Deeper/wider instruction windows**
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  - Load, store: consecutive storage

**Improved clock-gating**

- **Design & micro-arch efficiency**
- **Branch accuracy: less wasted work**
- **Fusion / gather: less units of work**
- **Reduced ports / access**
  - Sliced target reg-file
  - Reduced read ports / entry

P10 Core Micro-architecture

1/2 SMT8 Core Resources Shown = SMT4 Core Equivalent

Watt vs. POWER9: Improved
Powerful Core: Energy Efficient

- Double SIMD + Inference acceleration
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  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
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- Branch
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT
- Fusion
  - Fixed, SIMD, other: merge and back to back
  - Load, store: consecutive storage

- Improved clock-gating
- Design & micro-arch efficiency
- Branch accuracy: less wasted work
- Fusion / gather: less units of work
- Reduced ports / access
  - Sliced target reg-file
  - Reduced read ports / entry
- EA-tagged L1-D Cache & L1-I Cache
  - CAM with cache-way/index
  - ERAT only on cache miss

Watt vs. POWER9: Improved
Powerful Core: **Strength & Efficiency**

- **Double SIMD + Inference acceleration**
  - 2x SIMD, 4x MMA, 4x AES/SHA
- **Larger working-sets**
  - 1.5x L1-Instruction cache, 4x L2, 4x TLB
- **Deeper/wider instruction windows**
- **Data latency (cycles)**
  - L2 13.5 (minus 2), L3 27.5 (minus 8)
  - L1-D cache 4 +0 for Store forward (minus 2)
  - TLB access +8.5 (minus 7)
- **Branch**
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT
- **Fusion**
  - Fixed, SIMD, other: merge and back to back
  - Load, store: consecutive storage

- **Improved clock-gating**
- **Design & micro-arch efficiency**
- **Branch accuracy: less wasted work**
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IBM POWER10

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**P10 Core Micro-architecture**

½ SMT8 Core Resources Shown = SMT4 Core Equivalent

- **Fetch / +Branch Predictors**
- **Instruction Buffer**
  - 128 entries
- **Instruction Table**
  - 512 entries
- **MMA Accelerator**
  - 2x512b
- **Execution Slice**
  - 128b
- **Store Queue**
  - 80 entries (SMT), 40 entries (ST)
- **Load Queue**
  - 128 entries (SMT), 64 entries (ST)
- **Load Miss Queue**
  - 12 entries
- **Prefetch**
  - 16 streams
- **L1 Data Cache**
  - 32k 8-way
- **L1 Instr. Cache**
  - 48k 6-way
- **Instruction Table**
  - 512 entries
- **Execution Slice**
  - 128b
- **Execution Slice**
  - 128b
- **Execution Slice**
  - 128b
- **Execution Slice**
  - 128b
- **2 Load EA**
- **2 Store EA**
- **32B LD**
- **32B LD**
- **Load Miss Queue**
  - 12 entries
- **Prefetch**
  - 16 streams
- **ERAT**
  - 64 entry
- **L1 Data Cache**
  - 32k 8-way
- **Load Queue**
  - 128 entries (SMT), 64 entries (ST)
- **Store Queue**
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  - 16 streams
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  - 64 entry
- **L1 Data Cache**
  - 32k 8-way
- **L2 Cache**
  - (hashed index)
- **L3 Prefetch**
  - 48 entries
Powerful Core: Strength & Efficiency

- Double SIMD + Inference acceleration
  - 2x SIMD, 4x MMA, 4x AES/SHA
- Larger working-sets
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  - L2 13.5 (minus 2), L3 27.5 (minus 8)
  - L1-D cache 4+0 for Store forward (minus 2)
  - TLB access +8.5 (minus 7)
- Branch
  - Target registers with GPR in main regfile
  - New predictors: target and direction, 2x BHT
- Fusion
  - Fixed, SIMD, other: merge and back to back
  - Load, store: consecutive storage

1.3x

= 2.6x performance / watt

POWER10 vs. POWER9 Core

- Improved clock-gating
- Design & micro-arch efficiency
- Branch accuracy: less wasted work
- Fusion / gather: less units of work
- Reduced ports / access
  - Sliced target reg-file
  - Reduced read ports / entry
- EA-tagged L1-D Cache & L1-I Cache
  - CAM with cache-way/index
  - ERAT only on cache miss
Powerful Core: AI Infused Bandwidth and Compute

2x Bytes from all sources
(OMI, L3, L2, L1 caches*)
Powerful Core: AI Infused Bandwidth and Compute

2x Bytes from all sources (OMI, L3, L2, L1 caches*)

- 4 32B loads, 2 32B stores per SMT8 Core
  - New ISA or fusion
  - Thread max 2 32B loads, 1 32B store

* versus POWER9
Powerful Core: AI Infused Bandwidth and Compute

2x Bytes from all sources
(OMI, L3, L2, L1 caches*)

- 4 32B loads, 2 32B stores per SMT8 Core
  - New ISA or fusion
  - Thread max 2 32B loads, 1 32B store

- OMI Memory to one Core
  - 256 GB/s peak, 120 GB/s sustained
  - With 3x L3 prefetch and memory prefetch extensions

* versus POWER9
Powerful Core: AI Infused Bandwidth and Compute

2x Bytes from all sources
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2x Bandwidth matched SIMD*

• 8 independent SIMD engines per Core
  • Fixed, float, permute

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IBM POWER10
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**2x Bandwidth matched SIMD**
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**4-32x Matrix Math Acceleration**
- 4 512b engines per core = 2048b results / cycle
  - Matrix math outer products: \( A \leftarrow (\pm)A (\pm)XY^T \)
  - Double, Single, Reduced precision

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**Rank** | **Operand Type \((X,Y)\)** | **Accumulator** | **Peak [FLOPS] / cycle**
--- | --- | --- | ---
1 | Float-64 DP | 4x1 1x2 | 16 | 32 | 64
1 | Float-32 SP | 4x1 1x4 | 32 | 64 | 128
2 | Float-16 HP | 4x2 2x4 | 64 | 128 | 256
2 | Bfloat-16 HP | 4x2 2x4 | 128 | 256 | 512
4 | Int-8 | 4x4 4x4 | 256 | 512 | 1024
8 | Int 4 | 4x8 8x4 | 16B SIMD
16B SIMD
64B SIMD
64B SIMD
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* versus POWER9
AI Infused Core: Inference Acceleration

• 4x+ per core throughput
• 3x → 6x thread latency reduction (SP, int8)*

• POWER10 Matrix Math Assist (MMA) instructions
  • 8 512b architected Accumulator (ACC) Registers
  • 4 parallel units per SMT8 core

• Consistent VSR 128b register architecture
  • Minimal SW ecosystem disruption – no new register state
  • Application performance via updated library (OpenBLAS, etc.)
  • POWER10 aliases 512b ACC to 4 128b VSR’s
    • Architecture allows redefinition of ACC

• Dense-Math-Engine microarchitecture
  • Built for data re-use algorithms
  • Includes separate physical register file (ACC)
  • 2x efficiency vs. traditional SIMD for MMA

* versus POWER9
POWER10 SIMD / AI Socket Performance Gains

Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering.
**POWER10: Built for the Enterprise Cloud**

**Data Plane Bandwidth, Capacity, Composability, Scale**
Unparalleled Flexibility Ranging from Mission-Critical-Large-Scale to Purpose-Built-Systems to Cloud-Datacenter

**Powerful Enterprise Core**
Strong Foundation for Enterprise-grade Performance, Scale, and Resiliency

**End-to-End Security**
POWER10 + PowerVM = Reliable, Secure Protection of Enterprise Assets: End-to-End, All the Time

**Energy Efficiency**
Greener Data Centers for a Cleaner Planet: 3x improvement over POWER9

**AI-Infused Core**
Supercharging the Enterprise with AI Inferencing: 10-20x POWER9 capability

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