A 3.2 Gbps/pin HBM2E PHY with Low Power I/O and Enhanced Training Scheme for 2.5D System-in-Package Solutions

Sangyun Hwang, Kwanyeob Chae, Taekyung Yeo, Sangsoo Park, Won Lee, Shinyoung Lee, Soo-Min Lee, Kihwan Seong, Eunkyoung Ha, Eunsu Kim, Jihun Oh, Kyoung-Hoi Koo, Sanghune Park, Jongshin Shin

Foundry Business, Samsung Electronics, Korea
Abstract

- **3.2 Gbps/pin HBM2E PHY IP implementation**
  - Low power I/O scheme (1.07 pJ/bit@write operation)
    - Minimize the number of blocks using VDDQ power
  - Training scheme using redundancy bits (~7% VWM gain)
    - Redundancy pins are used as candidates@initial training

\[ \hat{x}_{excluded,DQ}(i) = \arg\min_{x_i} VWM(DQ(x_i)), \quad i = 0, \ldots, 63 \]
Outline

- **Introduction**
  - HBM introduction and test chip for HBM2E PHY

- **Low power I/O**
  - Structure of driver and receiver

- **Training scheme considering redundancy pins**
  - Training flow chart

- **Measurement Results**
  - Implementation and power measurement results
  - Valid window margin results
Introduction

- **HBM2E (High Bandwidth Memory)** [1,2]
  - 1024 pins@>2.8Gbps (>358.4GB/s), 128bit/channel, 32bit/DQS
  - 8CH/device (VDDQ (1.2V), VDDC(1.2V))
  - # of stack/chip: 4H/8H
  - Application: HPC, Server
Test chip for HBM2E PHY

- Test chip structure
  - Two test chips and one HBM memory chip are integrated on single silicon interposer
  - Test chip includes one HBM2 PHY for 4CH and test logics such as traffic generator and memory controllers
  - Traffic generator has several DMAs and one RTIC*

* RTIC (Run Time Integrity Checker)
Outline

- **Introduction**
  - HBM introduction and test chip for HBM2E PHY

- **Low power I/O**
  - Structure of driver and receiver

- **Training scheme considering redundancy pins**
  - Training flow chart

- **Measurement Results**
  - Implementation and power measurement results
  - Valid window margin results
Low power I/O

- Minimize the number of blocks using VDDQ power by moving level shifter (LS) from input side of pre-driver to output side [3]
- Receiver uses only VDD power and it is designed to minimize the number of stages (2stage)

## Training scheme including redundancy pins

Motivation is to reduce performance variation among DQ pins which can be caused by PI (Power Integrity) and SI (Signal Integrity).

- Main idea is to include redundancy pins when performing training even though there are no defects.

\[
\hat{x}_{\text{excluded,DQ}}(i) = \arg\min_{x_i \in [0, 15]} VWM(DQ(x_i)), \quad i = 0, ..., 63
\]
Outline

- Introduction
  - HBM introduction and test chip for HBM2E PHY

- Low power I/O
  - Structure of driver and receiver

- Training scheme considering redundancy pins
  - Training flow chart

- Measurement Results
  - Implementation and power measurement results
  - Valid window margin results
Implementation results

- Test chip size is 5 x 3.55 mm² and implemented with 7nm fabrication process
- Two chips and one HBM memory are integrated on single interposer
- Except for training block, HBM PHY with IO for 4CH is 1.6 x 3 mm²
Power and VWM measurement results

- 1.07 pJ/bit @ write operation (HM and I/O)

<table>
<thead>
<tr>
<th>0.75V/1.2V/8CH</th>
<th>WRITE</th>
<th>READ</th>
<th>IDLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>HM</td>
<td>810</td>
<td>1480</td>
<td>36</td>
</tr>
<tr>
<td>I/O</td>
<td>2700</td>
<td>1130</td>
<td>14</td>
</tr>
</tbody>
</table>

Energy [pJ/b] 1.07 0.56 0.02

- Approximately 7% VWM enhancement
Conclusion

- **3.2Gbps/pin HBM2E PHY is implemented in 7nm**
  - PHY is verified on 2.5 SiP test chip

- **Low power I/O**
  - Minimize the number of blocks using VDDQ

- **Performance**
  - Training scheme including redundancy pins

- **1.07pJ/bit@WRITE and 7% VWM enhancement**